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Masterson

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[54] **PROGRAMMABLE MEMORY STATE MACHINE FOR PROVIDING VARIABLE CLOCKING TO A MULTIMODE MEMORY**

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[51] **Int. Cl.**[5] **H03K 3/017**

[52] **U.S. Cl.** **307/480**; 307/265; 307/269; 328/58; 364/200; 365/233; 365/238.5

[58] **Field of Search** 307/443, 465, 480–481, 307/265, 269; 328/58, 63; 364/270.2, 950.4; 365/233, 238.5

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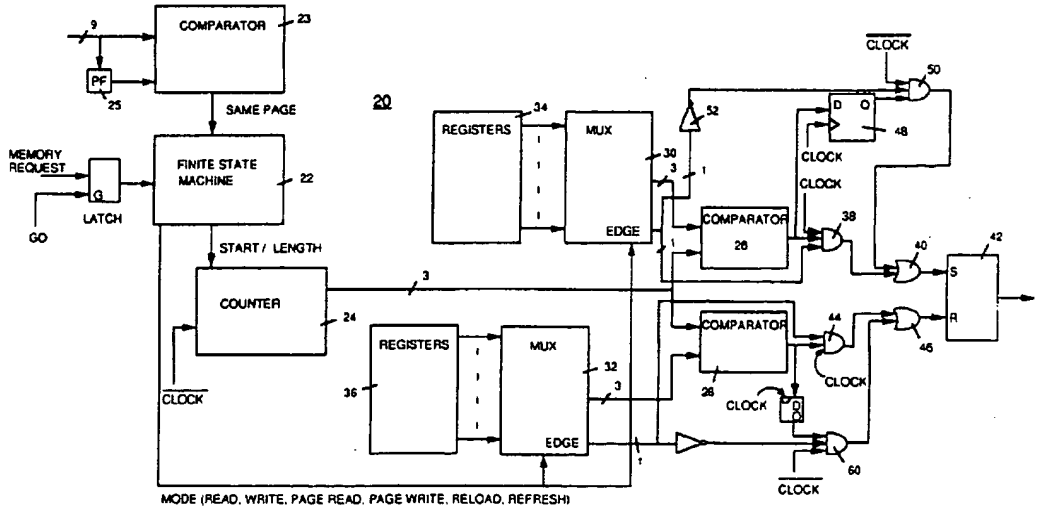
[57] **ABSTRACT**

A circuit for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse, the circuit comprising apparatus for providing signals indicating a mode of operation for access to a matrix of memory elements, apparatus responsive to the signals provided by the apparatus for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence, and apparatus responsive to the signals provided by the apparatus for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate.

12 Claims, 4 Drawing Sheets



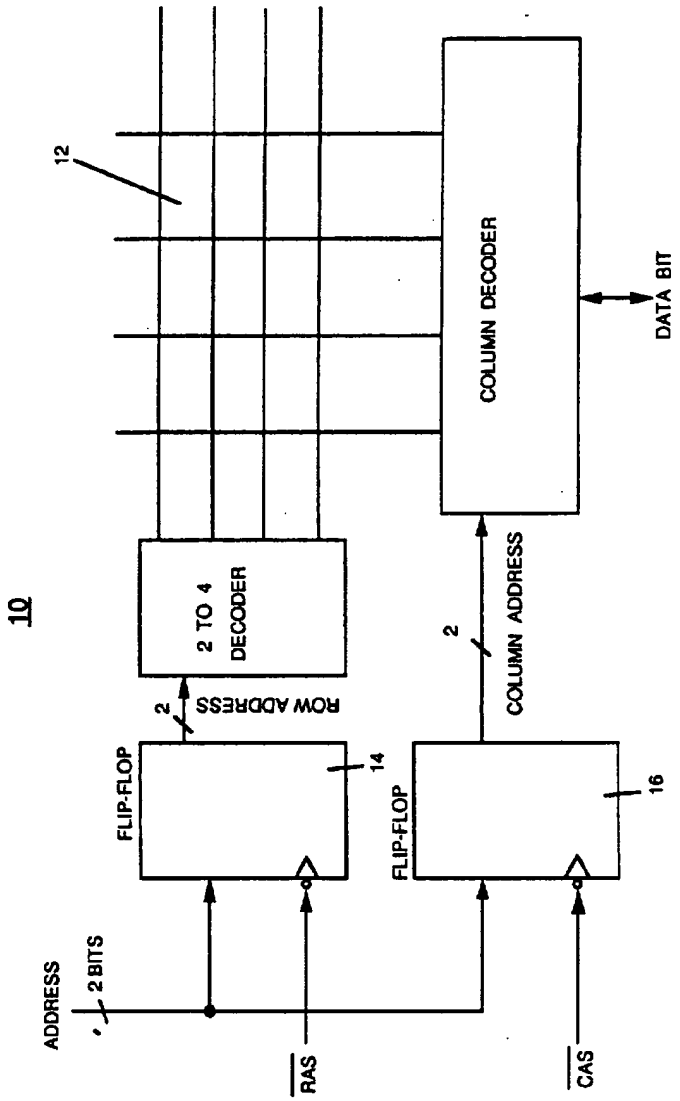

10
12
COLUMN DECODER
DATA BIT
2 TO 4 DECODER
2
ROW ADDRESS
2
COLUMN ADDRESS
FLIP-FLOP
14
FLIP-FLOP
16
ADDRESS
2 BITS
RAS
CAS

FIGURE 1

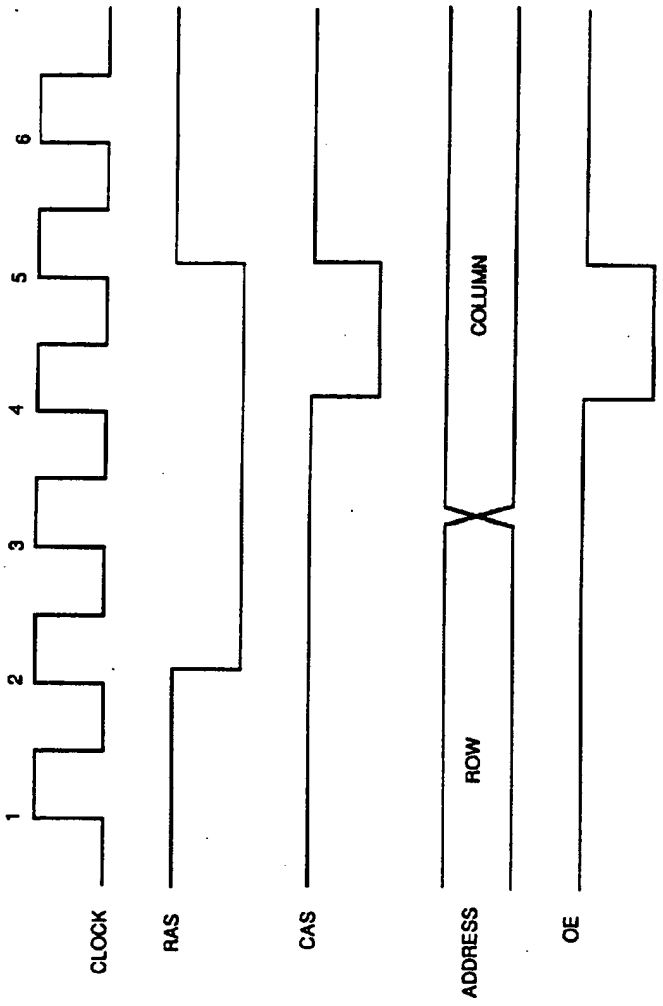


FIGURE 2

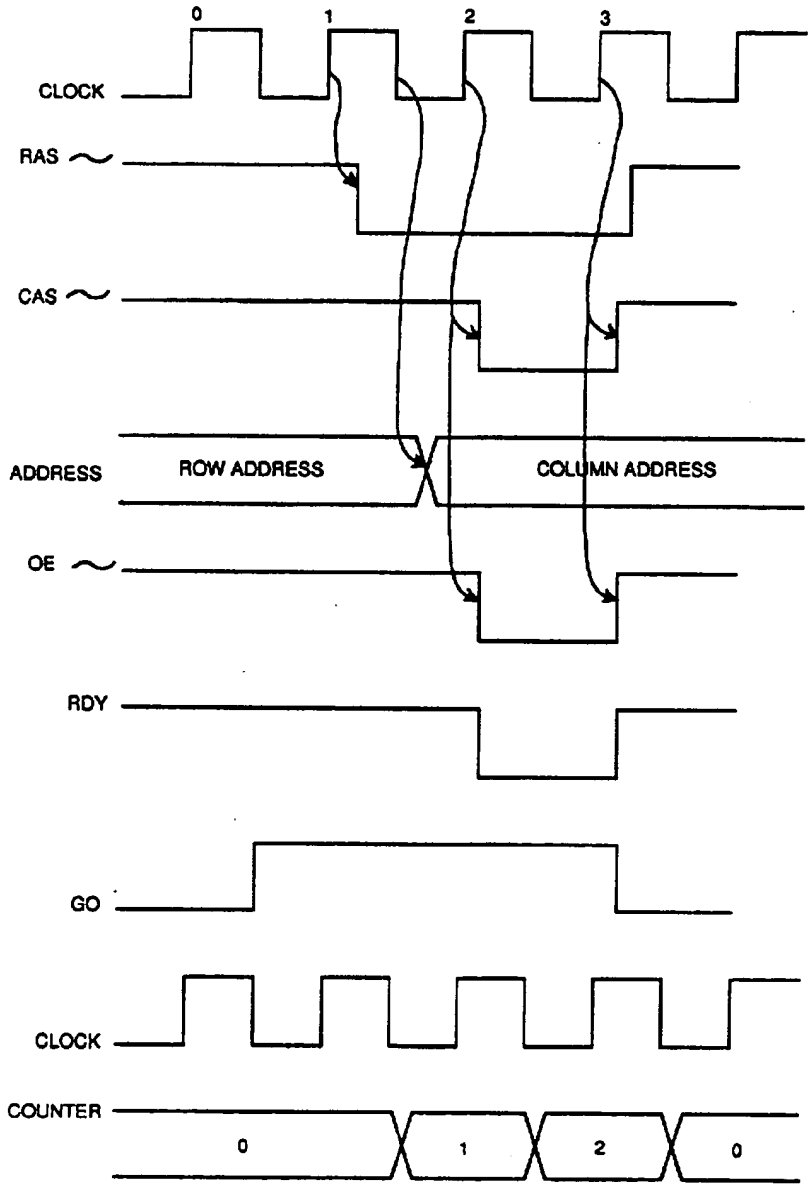

0
1
2
3
CLOCK
RAS
CAS
ADDRESS
ROW ADDRESS
COLUMN ADDRESS
OE
RDY
GO
CLOCK
COUNTER
0
1
2
0

FIGURE 3

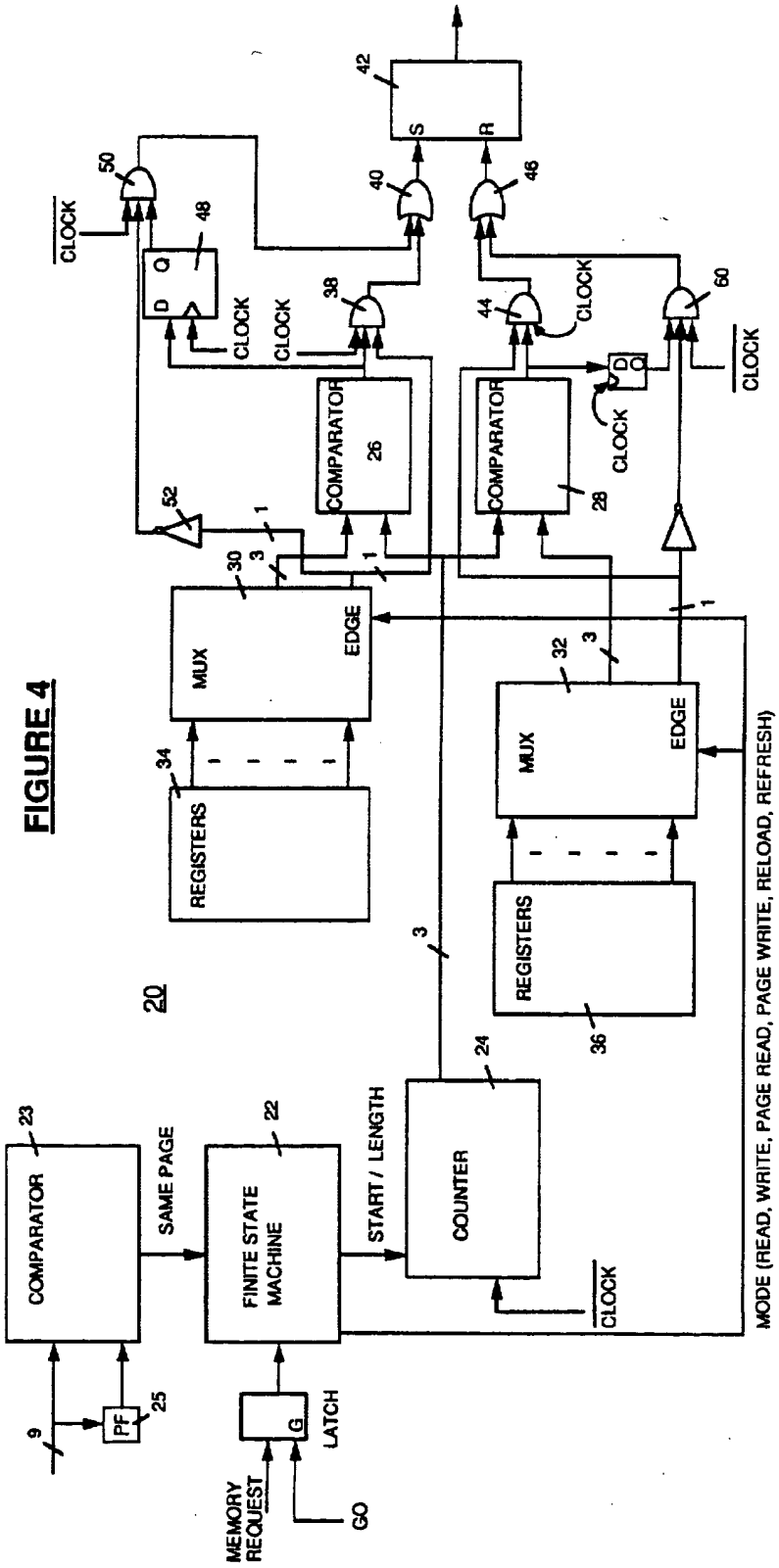

42
S
R
50
40
46
CLOCK
48
D
Q
CLOCK
CLOCK
38
44
CLOCK
60
CLOCK
COMPARATOR
26
COMPARATOR
28
CLOCK
52
30
3
1
1
MUX
EDGE
32
3
1
MUX
EDGE
34
REGISTERS
REGISTERS
36
3
20
24
23
22
COMPARATOR
SAME PAGE
FINITE STATE MACHINE
START / LENGTH
COUNTER
CLOCK
MODE (READ, WRITE, PAGE READ, PAGE WRITE, RELOAD, REFRESH)
9
PF
25
G
LATCH
MEMORY REQUEST
GO

FIGURE 4

PROGRAMMABLE MEMORY STATE MACHINE FOR PROVIDING VARIABLE CLOCKING TO A MULTIMODE MEMORY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to computer memory systems, and, more particularly, to arrangements for selectively varying the length of control signals used in a computer memory arrangement.

2. History of the Prior Art

In a conventional computer memory system utilizing dynamic random access memory (DRAM) elements, any particular memory position is accessed by providing a row address and a column address with corresponding row address strobe and column address strobe signals each occurring at a particular time and having a particular length sufficient to select the memory position for the particular mode of operation and for the particular type of memory element being used.

Any particular memory system may be constructed of DRAM elements (or VRAM elements) all capable of switching at a particular switching speed such as 150 nanoseconds, 120 nanoseconds, or 80 nanoseconds. In the memory system any particular computer, it is desirable to be able to utilize DRAM elements having different switching times. To utilize DRAMs having different switching times in the same memory system, the control pulses such as the row address strobe and the column address strobe must therefore either be sufficiently long and occur at sufficient intervals that they may be utilized with the slowest switching DRAM elements expected to be used with the system or the system must be somehow capable of switching the times and intervals between such control pulses in some manner to match the particular switching elements to be used. If the control pulses and intervals therebetween are selected to be long enough to handle the slowest switching memory elements, then the system will run at a relatively slow speed even with memory elements capable of switching at much higher speeds. To obviate this problem, it is desirable to be able to reprogram the memory controller to take advantage of the faster access time if faster memory is inserted into the system.

Even a memory system capable of using only memory elements which operate at a single speed, may be made substantially faster if its control signals may be programmed to match the speeds of the particular modes of operation. For example, a read cycle and a write cycle may take entirely different times to accomplish. A read cycle and a page read cycle (one in which the same row address is used for adjacent memory positions so that a new page need not be addressed) should take different times to accomplish. However, unless the control signals may be varied to fit the length of the these particular modes of operation, the differences in speed available to the different modes will not in practice be carried through to the operation of the machine.

For these reasons, attempts have been made to provide programmable length control signals for effecting the operation of computer memory systems. Programmable length control signals have been realized to some extent, but the arrangements provided to date have been able to program such memory signals to select only between control signals which both begin and end on a single edge of a clock pulse (the rising edge). For this reason, the length of control pulses and the intervals

therebetween have not been ptimized both to match the switching times of the memory elements where those switching times may vary from unit to unit and to match the particular modes of operation being practiced by the machine.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to speed the operations of computer memory systems.

It is another object of the present invention to provide apparatus capable of being programmed to furnish variable length control signals which may commence and end on either the leading or trailing edge of the clock pulses driving the particular arrangement.

It is an additional object of the present invention to provide computer memory systems, the control signals for which may be programmed in length and in interval to match the memory elements used in the system and the mode of operation of the system.

This and other objects of the present invention are accomplished by a circuit for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse, the circuit comprising means for providing signals indicating a mode of operation for access to a matrix of memory elements, means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence, and means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate.

These and other objects and features of the invention will become apparent to those skilled in the art by reference to the following detailed description taken together with the drawings in which like elements are referred to by like designations throughout the several views.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1, illustrates in simplified form a typical addressing system for a computer DRAM memory.

FIG. 2 illustrates the timing of the various signals provided in order to accomplish a particular access in prior art systems.

FIG. 3 illustrates the timing of various signals in a particular memory control system in accordance with the invention in which the length of the row address strobe and the column address strobe may be programmed.

FIG. 4 illustrates an arrangement in accordance with the present invention by which programmable control signals may be provided for operating a memory matrix.

NOTATION AND NOMENCLATURE

Some portions of the detailed descriptions which follow are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art.

An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary or desirable in most cases in any of the operations described herein which form part of the present invention; the operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases the distinction between the method operations in operating a computer and the method of computation itself should be borne in mind. The present invention relates to apparatus and to method steps for operating a computer in processing electrical or other (e.g. mechanical, chemical) physical signals to generate other desired physical signals.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIG. 1, there is shown in simplified form a typical addressing system 10 for a computer DRAM memory. The system 10 includes a memory arrangement 12 of four rows and four columns of memory elements arranged in matrix form. It should be assumed that the memory arrangement 12 includes a dynamic random access memory element at each intersection having connections made in a conventional manner. In order to select any particular memory element for access, a first row selection flip-flop 14 receives both a row address signal used to designate one of two particular rows with which it is associated and a row address strobe (RAS) pulse used to time the access. A second column selection flip-flop 16 receives a column address signal used to designate the selected column and a column address strobe (CAS) pulse used to time the access. The selection of the particular row and column addresses and the provision of the row address strobe signal and a column address strobe signal selects a particular memory element for access and the interval of the access.

FIG. 2 illustrates the timing of the various signals provided in order to accomplish a particular access. In FIG. 2 a read operation is assumed. The system clock signal is shown in the top line of FIG. 2. This signal, as is known to those skilled in the art, is utilized for timing the various signals such as the row address strobe and the column address strobe. These two signals are shown in FIG. 2 immediately following the system clock signal. In FIG. 2, the row address strobe and the column address strobe signals vary between positive five volts and zero volt conditions and are considered to be asserted in the zero volt condition.

As may be seen in FIG. 2, the address signal used in selecting the particular row of interest, (in this case row four), is provided during an interval which has begun before the first clock pulse illustrated and continues until the leading edge of the third clock pulse. At this time, the column address signal is provided and continues for a time the length of which is not pertinent to the present description. While the row address signal is present at flip-flop 14, the row address strobe pulse is asserted at the flip-flop 14 on the rising edge of the second clock pulse thereby effecting the selection of the particular row of the matrix 12. At the rising edge of the third clock pulse, the column address signal is provided to the flip-flop 16 so that the flip-flop 16 is in condition to receive the column address strobe. The column address strobe occurs at the rising edge of clock pulse four and continues to the rising edge of clock five. This causes the selection of the particular memory element of the matrix 12 to be accomplished, and the output enable signal OE is furnished during the period between the rising edge of clock pulse four and and the rising edge of clock pulse five so that the memory element is read.

It may be seen from FIG. 2 that the particular implementation of the typical DRAM control signals requires three cycles from the rising edge of clock cycle two to the rising edge of clock cycle five in order to accomplish the particular read operation. In many cases, the switching elements of the DRAM matrix 12 may be able to operate in a shorter time span than the interval provided by such control signals so that shortening the lengths of those control signals would provide faster system operation. Moreover, it may also be that more precise intervals of operation are desirable for the different modes of operation in which the access of the memory matrix 12 may be desired. For example, the time taken for a read, a write, a page read, a page write, or other memory operation may, and probably will, differ in any particular memory control arrangement. A system will operate more efficiently if the access time for each mode may be varied to precisely fit the interval needed for such mode. Consequently, it is desirable to be able to provide a system which is capable of providing selectable length control signals such as row access strobe, column access strobe, output enable,write enable, and address multiplexor control which may be varied depending on the particular switching time of the memory element to be used and the mode of operation of the memory circuitry. This desirable feature is difficult to accomplish in a memory system in which the control signals occur only on the rising edge of the clock pulse because all control signals must be an integer multiple of a clock pulse in length.

FIG. 3 is another timing diagram illustrating the time which may be saved in a particular memory control system in which the length of two of these control signals, the row address strobe and the column address strobe, may be programmed to occur upon either the rising or falling edge of a clock pulse. In the diagram illustrated in FIG. 3, the clock is shown at the top followed by the row address strobe signal. It may be seen that the row address strobe signal begins at the rising edge of the second clock pulse during the interval in which the row address signal is available at the flip-flop 14 shown in FIG. 1. Since the control signals are presumed to be programmable to occur upon either the rising or falling edges of a clock pulse, the address changes from row address to column address on the

falling edge of the second clock pulse rather than being required to wait for the rising edge of the third clock pulse. Consequently, at the rising edge of the third clock pulse, the column address strobe signal may occur to select the particular column address. At this same clock time, the output enable signal begins and continues until the rising edge of the fourth clock pulse at which point the row address strobe signal and the column address strobe signal both terminate.

Reviewing the intervals illustrated in FIG. 3, it is clear that the read operation illustrated therein takes but two clock cycles for its operation thereby conserving a clock cycle over the arrangement illustrated in FIG. 2 for accomplishing a read operation. Thus, a system implementing the timing illustrated in FIG. 3 may be made to operate essentially half again as fast as does the typical memory system.

FIG. 4 illustrates an arrangement in accordance with the present invention by which programmable control signals of variable lengths may be provided for operating a memory matrix such as that shown in FIG. 1. The control system 20 illustrated in FIG. 4 includes a finite state machine 22 which receives a memory request from a processor controlling its operation. The finite state machine 22 provides output signals indicating the mode of operation, the starting time, and the number of counts at one count per clock cycle to be provided for the particular mode of operation. It should be noted that the system also includes a comparator 23 which receives the row address for the selected memory position and compares this address with the row address of the last signal which is stored in a flip-flop 25. This comparison determines whether the addresses are both in the same page so that page read or page write mode access may be performed as appropriate.

The signals indicating the number of counts and the starting time of the count are used to initiate operation of a counter 24. The counter 24 is driven by a clock signal (in the present case a clock bar signal or signal of opposite polarity to the system clock pulse) in the preferred embodiment. The output of the counter 24 is furnished to a pair of comparators 26 and 28 each of which also receives an output signal from either a multiplexor 30 and 32. The multiplexor 30 is furnished a number of inputs from a set of registers 34 while the multiplexor 32 receives a number of inputs from a set of registers 36. The registers 34 and 36 each store information indicative of a particular count upon which an operation is to occur and the edge upon which the particular action is to occur. Each register of the registers 34 in the preferred embodiment stores four bits of information for one mode of memory access, three bits indicating the count upon which a control pulse is to commence and one bit indicating the edge of the clock upon which the commencement occurs (rising or falling).

The multiplexor 30 is enabled by a signal from the state machine 22 indicating the mode of operation of the memory array (read, write, page read, page write, or some other operation). Based on that mode signal, the multiplexor 30 selects from the registers 34 the count during which the leading edge of the particular control signal is to occur and the particular edge of the clock signal upon which that control signal is to take place. The count furnished by the multiplexor 30 is compared to the output of the counter 24 at a comparator 26; and when the counts coincide, produces an output signal which is furnished to and AND gate 38. The AND gate 38 also receives the system clock pulse and the edge signal from the multiplexor 30; and, when these three coincide, produces an output which is transferred by an OR gate 40 to set a set/reset flip-flop 42 and begin the particular control pulse. The set/reset flip-flop 42 is of a type which, once it has been placed in a particular condition such as set by a signal on the input set line, will remain in the set condition until reset by a signal on the reset line no matter what signals appear during the interim on the set line. In like manner, once reset by a signal on the reset line, the flip-flop 42 will remain reset until a set signal appears on the set line no matter what signals appear on the reset line.

In FIG. 3, for example, the leading edge of the row address strobe signal for a read access occurs following the rising edge of the second clock cycle. At this instant, the counter 24 is producing an output signalling a zero count, the count in which the row address strobe begins in FIG. 3.

Like the registers 34, each of the registers 36 in the preferred embodiment stores four bits of information defining the count and the clock edge. These are used, however, for terminating a control signal in one mode of operation of the memory. The multiplexor 32 also receives the mode signals from the state machine 22 to cause the selection of the trailing edge of the particular control signal causing signals from the selected one of the registers 36 to be furnished to the comparator 28. For example, in FIG. 3 the row address strobe signal ends at the rising edge of the third clock signal when the counter has reached two, and this would occur in the comparator 28 when the counter signal provided by counter 24 and the count signal provided by multiplexor 32 are equal. The output of the comparator 28 is furnished to an AND gate 44 which ANDs the system clock signal and the edge signal from the multiplexor 32 to produce a reset signal via an OR gate 46 to the set/reset flip-flop 42 and terminate the particular control signal.

In order to operate the system 20 illustrated in FIG. 4 to initiate or terminate a particular control signal on the falling edge of the clock pulse, the system 20 includes circuitry including a flip-flop 48 which receives the output of the comparator 26 and is driven by the system clock signal to furnish an output to an AND gate 50. The AND gate 50 receives the edge indication signal through an inverter 52 from the multiplexor 32 and the clock bar signal (a signal of polarity opposite the system clock signal). When these three signals coincide, an output is provided to the OR gate 40 to set the set/reset flip-flop 42.

The coincidence of the signals providing for timing based on the trailing edge of the clock pulse may be best illustrated by the read operation shown in FIG. 3 in which the read signal is initiated by the falling edge of the second clock pulse.

In operation, the system 20 receives a memory request at the finite state machine 22. The machine 22 provides a mode output signal to the multiplexors 30 and 32 and starts the operation of the counter by means of a start signal and length of count signal. The multiplexor 30 selects the appropriate register 34 to provide the count start signal and an edge for the start of the control signal for the particular mode. The comparator 26 compares the count and the count start signal furnished by the multiplexor 30 and produces an enabling output when they coincide. The enabling signal is furnished to the AND gates 38 and 50 where it is ANDed

with the system clock signal and the edge signal and with the clock bar signal and the inverted edge signal, respectively. The particular edge signal selects the appropriate AND gate 38 or 50 to produce an output to the OR gate 40 for setting the flip-flop 42 and starting the control signal.

In like manner, the multiplexor 32 selects the appropriate register 36 to provide the count start signal and an edge signal for the end of the control signal for the particular mode. The comparator 28 compares the count and the count end signal furnished by the multiplexor 32 and produces an enabling output when they coincide. The enabling signal is furnished to the AND gates 44 and 54 where it is ANDed with the system clock signal and the edge signal and with the clock bar and the inverted edge signal, respectively. The particular edge signal selects the appropriate AND gate 44 or 60 to produce an output to the OR gate 46 for resetting the flip-flop 42 and ending the control signal. In this manner the starting and ending edges and the intervals of control signals such as the row address strobe, the column address strobe, the output enable, write enable, and address multiplexor control signals may be precisely programmed to enhance the speed of operation of the particular computer system.

Although only a few examples have been given to illustrate the operation of the circuit of the invention, it will be obvious that control signals may be selectively varied depending on the particular mode of operation desired for the circuitry as well as the particular switching times of which the memory elements are capable. Consequently, the circuitry illustrated in FIG. 4 is capable of providing much faster operation times for memory switching than are prior art arrangements.

Although the invention has been described with reference to particular arrangements and computer systems, it will be apparent to those skilled in the art that the details of those arrangements and systems are used for illustrative purposes and should not be take as limitations of the invention. It is, thus, to be contemplated that many changes and modifications may be made by those of ordinary skill in the art without departing from the scope and spirit of the invention.

What is claimed is:

1. A circuit for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse, the circuit comprising means for providing signals indicating a mode of operation for access to a matrix of memory elements, means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence, and means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate.

2. A circuit as claimed in claim 1 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence comprises a means for storing a plurality of signals indicating clock periods and clock edges for a plurality of modes of operation, means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode, means for comparing a signal indicating a clock period for a mode with actual clock periods, and means for comparing a signal indicating a clock edge for a mode with actual clock edges.

3. A circuit as claimed in calim 2 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means for comparing a signal indicating a clock period for a mode with actual clock periods comprises a counter for furnishing signals indicating clock periods, a comparator circuit for comparing signals furnished by the counter with signals furnished by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period, and means responsive to the comparator circuit for providing a signal indicating that the clock period is correct.

4. A circuit as claimed in claim 2 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means for comparing a signal indicating a clock edge for a mode with actual clock edges comprises means for providing an output signal when a first clock edge and a first signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide; and means for providing an output signal when a second clock edge and a second signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide.

5. A circuit as claimed in claim 1 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate comprises means for storing a plurality of signals indicating clock periods and clock edges for a plurality of modes of operation, means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode, means for comparing a signal indicating a clock period for a mode with actual clock period, and means for comparing a signal indicating a clock edge for a mode with actual clock edges.

6. A circuit as claimed in claim 5 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means for comparing a signal indicating a clock period for a mode with actual clock periods comprises a counter for furnishing signals indicating clock periods, a comparator circuit for comparing signals furnished by the counter with signals furnished by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period, and means responsive to the comparator circuit for providing a signal indicating that the clock period is correct.

7. A circuit as claimed in claim 5 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means for comparing a signal indicating a clock edge for a mode with actual clock edges comprises means for providing an output signal when a first clock edge and a first signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide; and means for providing an output signal when a second clock edge and a second signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide.

8. A circuit as claimed in claim 1 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence comprises first means for storing a plurality of signals indicating clock periods and clock edges for a plurality of modes of operation, first means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode, first means for comparing a signal indicating a clock period for a mode with actual clock periods, and first means for comparing a signal indicating a clock edge for a mode with actual clock edges; and in which the means responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate comprises second means for storing a plurality of signals indicating clock periods and clock edges for a plurality of modes of operation, second means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode, second means for comparing a signal indicating a clock period for a mode with actual clock periods, and second means for comparing a signal indicating a clock edge for a mode with actual clock edges.

9. A circuit as claimed in claim 8 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which the first means for comparing a signal indicating a clock period for a mode with actual clock periods comprises a counter for furnishing signals indicating clock periods, a first comparator circuit for comparing signals furnished by the counter with signals furnished by the first means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period, and first means responsive to the comparator circuit for providing a signal indicating that the clock period is correct; and in which the second means for comparing a signal indicating a clock period for a mode with actual clock periods comprises the counter for furnishing signals indicating clock periods, a second comparator circuit for comparing signals furnished by the counter with signals furnished by the second means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period, and second means responsive to the the comparator circuit for providing a signal indicating that the clock period is correct.

10. A circuit as claimed in claim 8 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse in which each of the first and second means for comparing a signal indicating a clock edge for a mode with actual clock edges comprises means for providing an output signal when a first clock edge and a first signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide; and means for providing an output signal when a second clock edge and a second signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide.

11. A circuit for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse comprising means for providing signals indicating a mode of operation for access to a matrix of memory elements, a first plurality of registers for storing signals indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence, a first multiplexor responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals from the first plurality registers indicating a clock period during which a control signal is to commence and the edge of the clock signal at which such signal is to commence, a first comparator for comparing a signal indicating a clock period for a mode with actual clock periods, and first means for comparing a signal indicating a clock edge for a mode with an actual clock edge; and

a second plurality of registers for storing signals indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate, a second multiplexor responsive to the signals provided by the means for providing signals indicating a mode of operation for providing signals from the second registers indicating a clock period during which a control signal is to terminate and the edge of the clock signal at which such signal is to terminate, a second comparator for comparing a signal indicating a clock period for a mode with actual clock periods, and second means for comparing a signal indicating a clock edge for a mode with an actual clock edge.

12. A circuit as claimed in claim 11 for providing control signals of selectable lengths capable of being driven off of either the rising or falling edge of a clock pulse comprising in which the first and second means for comparing a signal indicating a clock edge for a mode with an actual clock edge each comprises means for providing an output signal when a first clock edge and a first signal indicating a clock edge provided by the multiplexor for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide; and means for providing an output signal when a second clock edge and a second signal indicating a clock edge provided by the means for selecting from the plurality of signals depending on the mode of operation to provide signals indicating a clock period and a clock edge for each mode coincide.

* * * * *

US005986491A

United States Patent [19]

Grehl et al.

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[45] Date of Patent: Nov. 16, 1999

[54] CLOCK SIGNAL GENERATOR

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[21] Appl. No.: **09/188,046**

[22] Filed: **Nov. 6, 1998**

Related U.S. Application Data

[63] Continuation of application No. PCT/DE97/00775, Apr. 17, 1997.

[51] **Int. Cl.**[6] **H03H 11/16**

[52] **U.S. Cl.** **327/239**; 327/175; 327/250

[58] **Field of Search** 327/239, 250, 327/251, 256, 257, 258, 259, 171, 172, 173, 174, 175, 176, 291, 295

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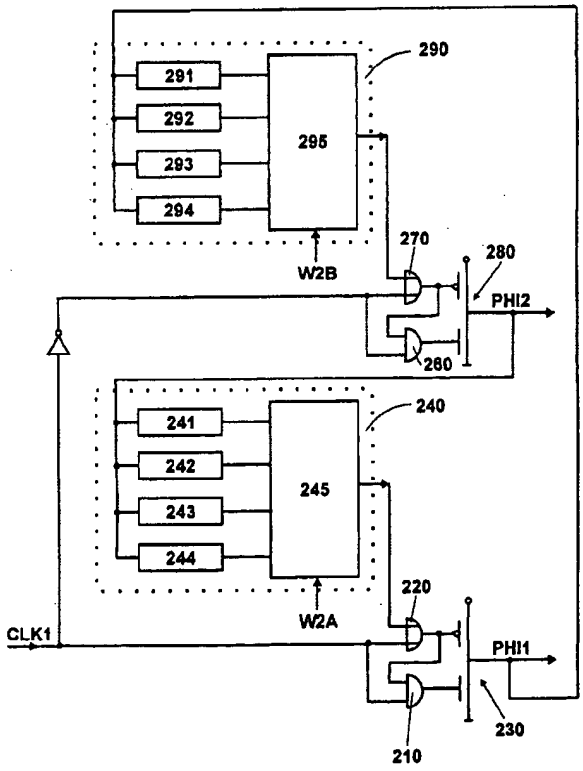
[57] **ABSTRACT**

The clock signal generator can be used to generate a first and/or a second output clock signal from an input clock signal. The rising and/or falling edges of the input clock signal are shifted using delay stages. The clock signal generator has a delay stage with a plurality of delay elements that are wired up in parallel and that have different delay lengths, and a selection device that is used to determine which of the output signals from the delay elements is to be output as the output signal of the delay stage.

6 Claims, 2 Drawing Sheets



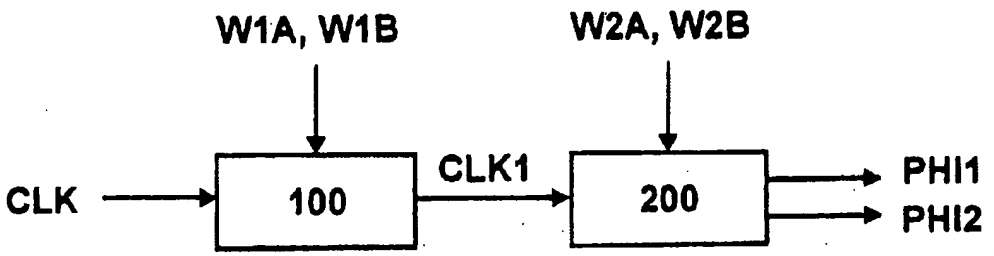

W1A, W1B
W2A, W2B
CLK
100
CLK1
200
PHI1
PHI2

FIG 1

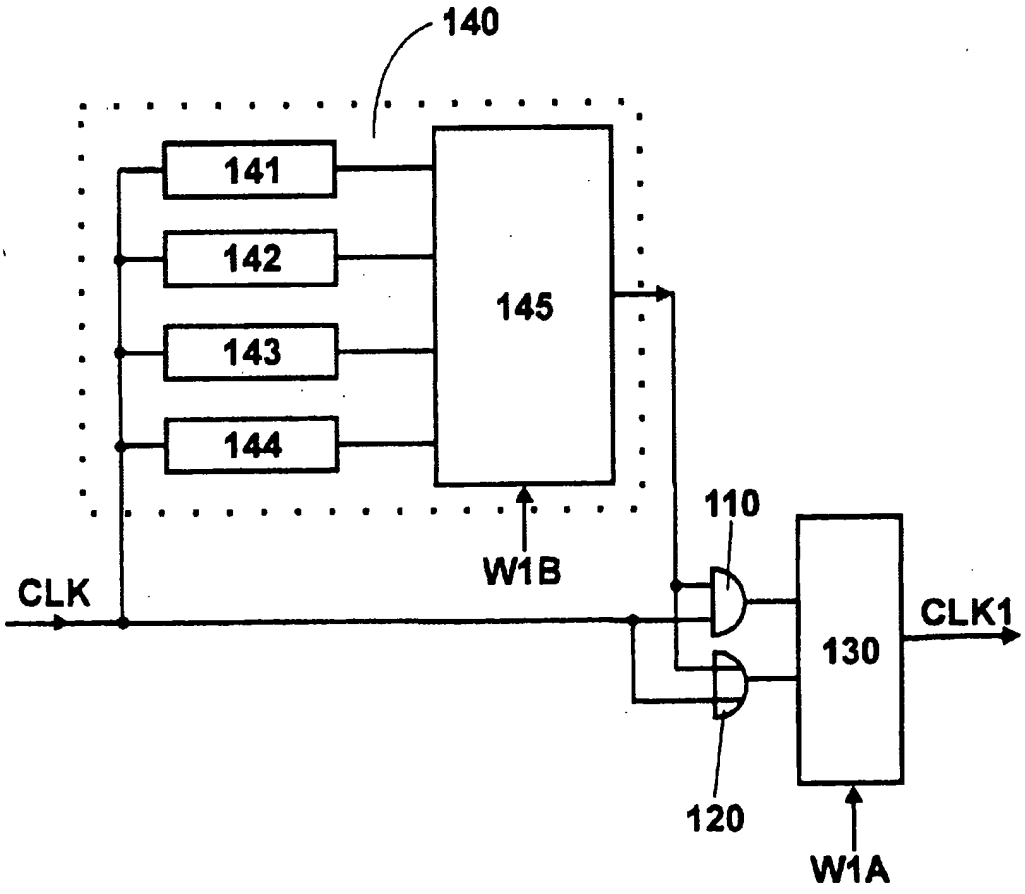

140
141
142
143
144
145
W1B
110
CLK
CLK1
130
120
W1A

FIG 2

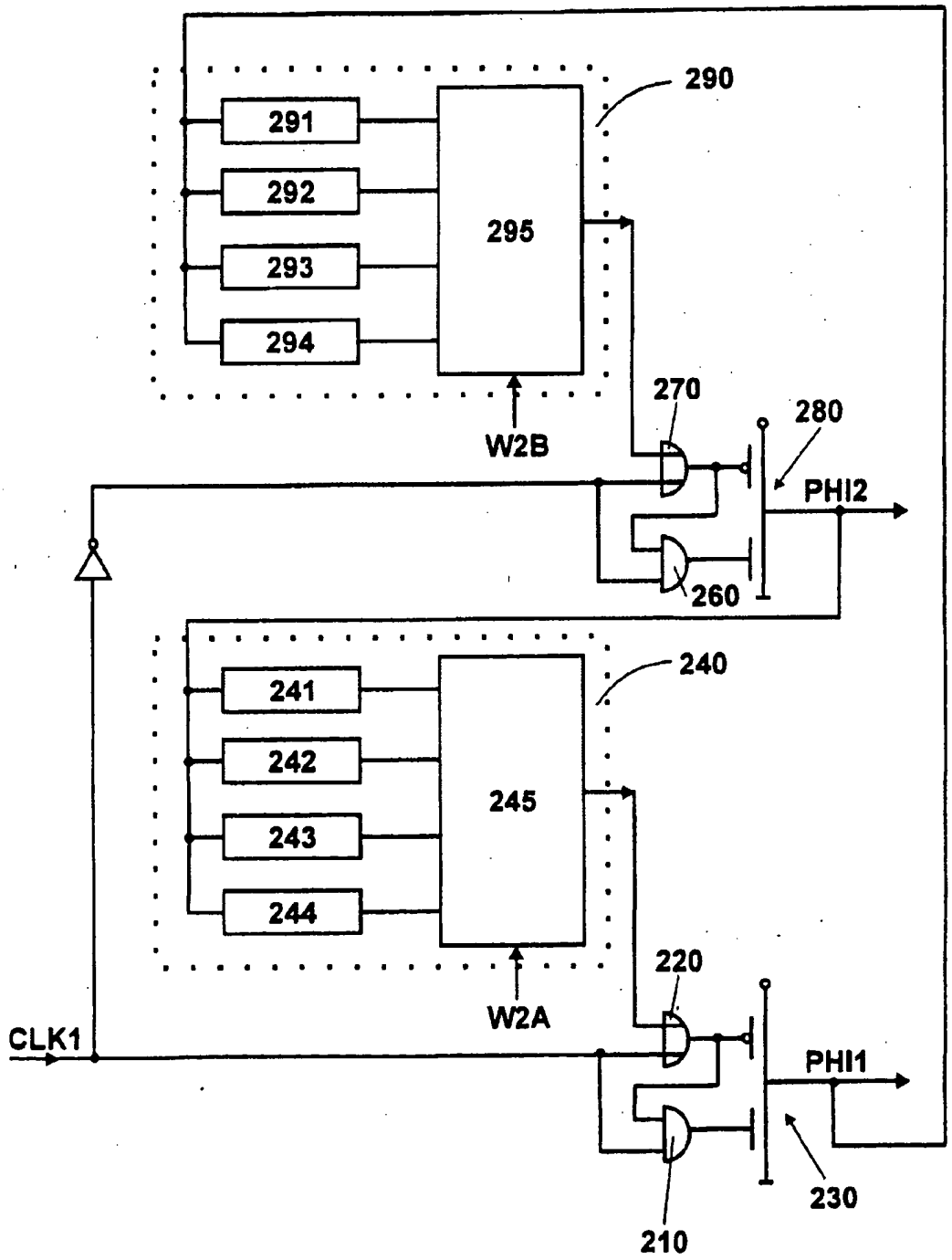

290
291
292
293
294
295
W2B
270
280
PHI2
260
240
241
242
243
244
245
W2A
220
CLK1
PHI1
230
210

FIG 3

CLOCK SIGNAL GENERATOR

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of copending International Application PCT/DE97/00775, filed Apr. 17, 1997, which designated the United States.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention lies in the electronics field. Specifically, the present invention relates to a clock signal generator in which the duty ratio of the clock signals produced is programmable.

A clocked logic circuit has been disclosed, for example, in U.S. Pat. No. 4,719,365 to Misono (European EP 0 183 875 A). That device, however, is not suitable for producing clock signals of the type to which the invention pertains.

Clock signal generators of the known type are used, amongst other things, for controlling master/slave registers and the like, for example. Master/slave registers contain two storage elements connected in series, namely a so-called master store and a so-called slave store, which are controlled using two mutually different clock signals. More precisely, the first clock signal determines the instant at which any data present are transferred to the master store, and the second clock signal determines the instant at which data stored in the master store are transferred to the slave store.

Data may generally be transferred from the master store to the slave store only when the clock signal controlling the master store has assumed a state which prevents data from being written to the master store. If this were not the case, the data stored in the master store would still be able to change while being transferred to the slave store, which should normally be avoided if possible.

Consequently, the first clock signal and the second clock signal must never simultaneously be in a state which allows data to be transferred to the respective store. This can be achieved, for example, by generating the second clock signal by inversion of the first clock signal, so that the clock signals have essentially complementary waveforms. Clock signals generated in this manner are, in principle, suitable for controlling master/slave systems and the like.

However, on account of signal delay times, component tolerances, and the like, the above-mentioned overlaps in the signal waveforms, which are to be avoided, may nevertheless occur with the clock signals. This is undesirable and a serious problem, particularly at high clock frequencies and with stores responding at a correspondingly fast rate.

In order to avoid this, it is possible to process the mutually inverse clock signals in such a manner that a so-called overlap-free phase is imposed between the respective active phase of one clock signal and the subsequent active phase of the other clock signal. Both clock signals are in an inactive phase, for example a low-level phase, during the overlap-free phase.

Such an overlap-free phase can be provided (while maintaining the respective clock frequencies) by appropriately shifting the rising and/or falling edges of the first and/or of the second clock signal. This can be achieved using appropriate delay stages. See, for example, U.S. Pat. No. 5,453,707 to Hikichi (European EP 0 606 912 A).

Even though the use of such clock signals matched to the supposed conditions generally permits master/slave registers and the like to be driven considerably more reliably, there are nevertheless repeatedly cases, in practice, in which master/slave registers or the like cannot be operated correctly, despite the provision of the measures. This necessitates research into the cause and requires the relevant circuit or its affected circuit parts to be redesigned, which processes are frequently very extensive and correspondingly costly.

The same also applies to the case where the duty ratio of the clock signals used is responsible for the master/slave registers or the like operating incorrectly. In that case, too, matching to the supposed conditions does not automatically lead to the correct operation of the master/slave registers.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide a clock signal generator, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which allows the proper and correct operation of master/slave registers or the like which are controlled by the clock signals of the clock signal generator at all times.

With the foregoing and other objects in view there is provided, in accordance with the invention, a clock signal generator, comprising:

a clock input;

a first logic configuration having an input receiving an intermediate clock signal and outputting a first clock output signal;

a second logic configuration having an input receiving the intermediate clock signal and outputting a second clock output signal;

the first and second clock signals having a programmable duty ratio and a programmable overlap-free time;

a first delay stage with a selectable delay connected to receive the second clock output signal and to supply the second clock output signal to the first logic configuration;

a second delay stage with a selectable delay connected to receive the first clock output signal and to supply the first clock output signal to the second logic configuration;

a third delay stage with a selectable delay, the third delay stage having an input connected to the clock input; and

a third logic configuration having an input connected to the clock input and outputting the intermediate clock signal to the input of the first logic configuration and to the input of the second logic configuration.

In accordance with an added feature of the invention, a multiplexer selects a delayed signal. The multiplexer is connected to a multiplicity of mutually parallel delay paths and it is controllable by an external control signal.

In accordance with an additional feature of the invention, a delayed signal is selectable by modifying a wiring of the multiplicity of parallel delay paths.

In accordance with another feature of the invention, a delayed signal is selectable by subsequently breaking wiring connections in the circuit with the multiplicity of parallel delay paths. The wiring connections are preferably broken by means of a laser beam.

In accordance with a concomitant feature of the invention, the third logic circuit has an AND gate and an OR gate each having a first input receiving the clock input signal and a second input receiving the signal delayed in the third delay stage, and wherein the intermediate clock signal is selectively tapped off at an output of the AND gate and an output of the OR gate.

In other words, the basic principle of the invention is found in the advantageous provision of a delay stage with a plurality of delay elements, which are wired up in parallel and have different delay lengths, and of a selection device which can be used to determine which of the output signals from the delay elements is to be output as the output signal of the delay stage.

This makes it possible to match, individually, the length of the active phases and of the inactive phases of the respective clock signals and the length of the overlap-free phases to the respective actual circumstances. These adjustments are possible even after the clock generator and the circuit to be driven by it have been produced, which means that the equipment which is to be driven by the clock signal generator according to the invention can be operated optimally in all cases.

If the clock signal generator according to the invention is used as a clock signal generator which is to be provided in an integrated circuit in order to drive the master/slave registers or the like which are also provided in the circuit, then malfunctioning of the integrated circuit—which is caused by the master/slave registers not being driven correctly and whose rectification, in the past, often required the integrated circuit to be completely redesigned—can frequently be eliminated simply by operating the clock signal generator, more specifically its delay stage(s) and/or its selection device(s), in an appropriately modified manner.

The invention thus provides for a clock signal generator by means of which master/slave registers or the like that are controlled by the clock signals of the clock signal generator can easily be operated correctly all the time.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a clock signal generator, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing the basic layout of an exemplary embodiment of the clock signal generator according to the invention;

FIG. **2** is a schematic block diagram illustrating a possible embodiment of the first block **100** shown in FIG. **1**; and

FIG. **3** is a schematic block diagram illustrating a possible embodiment of the second block **200** shown in FIG. **1**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1** thereof, there is seen a clock signal generator that comprises two blocks, namely a first block **100** and a second block **200**.

The task of the clock signal generator under consideration is to generate a first output clock signal PHI1 and a second output clock signal PHI2 from an input clock signal CLK. The output signals PHI1 and PHI2 drive a master/slave register or the like.

It will be understood by those skilled in the pertinent art that the use of the clock signal generator according to the invention is not restricted to the use described for driving master/slave registers and the like. Instead, the invention can be used wherever one or more clock signals are to be generated or provided which are in each case optimally matched to their application.

The first block **100** receives the input clock signal CLK as input signal and outputs an output signal (intermediate clock signal) CLK1, whose duty ratio is modified—if necessary—with respect to that of the input clock signal CLK. Whether and to what extent the original duty ratio is modified is determined by control signals W1A and W1B, which are input externally into the first block **100**. The internal design of the first block **100**. The effect of the control signals will be described in detail below with reference to FIG. **2**.

The second block **200** receives the output signal (intermediate clock signal) CLK1 from the first block **100** as input signal and outputs the first (PHI1) output clock signal and the second (PHI2) output clock signal as output signals. These signals having essentially complementary amplitude waveforms at first and—if necessary—are additionally modified in terms of the duration of the overlap-free phase already mentioned in the introduction. Whether and to what extent an originally non-existent overlap-free phase (in the case of signals with exactly complementary waveforms, the overlap-free phase is always equal to zero) is generated is determined by control signals W2A and W2B, which are input externally into the second block **200**. The internal design of the second block **200** and the effect of the control signals will be described in detail in the following text with reference to FIG. **3**.

The first block **100** will now be described in more detail with reference to FIG. **2**.

The first block comprises an AND gate **110**, an OR gate **120**, a first multiplexer **130** and a delay stage **140**, which are connected as shown in FIG. **2**.

The core element of the circuit shown in FIG. **2** is the delay stage **140**.

If this delay stage **140** were to be replaced by a continuous conduction element, the input signal CLK input into the first block **100** and the output signal CLK1 output from the first block would be entirely identical, specifically irrespective of whether the multiplexer **130**, which can be driven by the signal W1A, is outputting the output signal from the AND gate **110** or the output signal from the OR gate **120** as output signal CLK1. This is because, in this case, both the signals input into the AND gate **110** and the signals input into the OR gate **120** would be exactly identical at any chosen instant, namely the same as the input signal CLK input into the first block **100**.

In contrast to this, as a result of the delay stage **140** being provided, the AND gate **110** and the OR gate **120** can each receive one of their input signals offset in time, which, as can be seen, results in the rising or falling edges of the output signal CLK1 being shifted in time. In more precise terms, when the output signal from the AND gate **110** is used as the output signal CLK1 from the multiplexer **130** (and from the first block **100**), its edges are shifted in such a manner that the signal rises to the high level later or drops to the low level sooner than is the case with the input signal CLK, which results in the high-level phase being shortened (the low-level phase being lengthened), i.e. the duty ratio is changed. On the other hand, when the output signal from the OR gate **120** is used as the output signal CLK1 from the multiplexer **130** (and from the first block **100**), its edges are

shifted in such a manner that the signal rises to the high level sooner or drops to the low level later than is the case with the input signal CLK, which results in the high-level phase being lengthened (the low-level phase being shortened), i.e. the duty ratio is likewise changed.

The extent to which the duty ratio is changed is determined by the extent of the delay by the delay stage **140**. According to the invention, the latter is thus designed in such a way that it has a multiplicity of delay elements **141** to **144**, connected in parallel, and a selection device in the form of a second multiplexer **145**. The plurality of delay elements **141** to **144** are designed in such a way that they can be used to produce delays, for the signals input in each case, which can be defined as required but which are different from one another; in so doing, it may also be permitted for a delay to be equal to zero, that is to say for there to be no delay. All the delay elements receive one and the same input signal, namely the input clock signal CLK. This signal is delayed by the respective delay element according to the respective delay, but is output otherwise unchanged as the respective output signal from the respective delay element. The output signals from all delay elements **141** to **144** are input into the multiplexer **145**.

The multiplexer **145** can be used to select or determine, as a function of the control signal W1B supplied externally, which of the signals input into the multiplexer **145** is to be output as the output signal of the latter (and at the same time of the delay stage **140**).

The control signals W1A and W1B introduced externally into the first block **100** or into its multiplexers **130** and **145** thus enable the duty ratio of the input clock signal CLK to be set or purposefully changed, specifically both with regard to type (control signal W1A) and with regard to extent (control signal W1B).

The control signals W1A and W1B, i.e., their waveforms and/or values, may be stored in a memory unit, such as a register or the like, or may be permanently set by means of corresponding wiring.

Storage in a register or the like has the advantage that the corresponding values can then be (dynamically) changed at any time, that is to say even during operation. This enables particularly flexible matching to the respective circumstances, which is of considerable importance—particularly when taking account, as may be necessary, of conditions which vary with time, such as temperature, aging etc.—and, furthermore, also permits, among other things, automatic clock signal setting as part of a self-test of the circuit when it has been switched on or the like. The measures to be provided for storing appropriate initial values or updated values in the register or the like and the measures for using them as control signals W1A and W1B are known to those of skill in the art and do not require any further explanation.

Defining the control signals in such a way that they cannot subsequently be changed, for example by means of appropriate wiring, eliminates possible sources of error (by programming the clock signal setting incorrectly), protects against tampering and, under some circumstances, simplifies driving of the clock generator. One possibility for defining control signals in this manner in practice consists in destroying wiring which corresponds to unwanted clock signal settings and which is initially, i.e. after production of the relevant circuit or the relevant circuit part, still present intact. The appropriate connections may be broken, for example, using a laser beam, and should in this case be located at an easily accessible point. Another possibility for defining, in practice, the control signals such that they cannot subsequently be changed consists in omitting the connections which correspond to the unwanted clock signal settings as early as during the production stage; any changes which are subsequently found to be necessary can then be made with a minimum of effort (replacement of one connection with another), provided that the possibility of such modifications being needed was duly taken into account when the circuit was designed. A further possibility for defining, in practice, the control signals such that they cannot be changed consists in using a (if required, erasable) read-only memory (ROM, PROM, EPROM, EEPROM, flash EPROM) as a storage device for storing the waveforms and/or values for the control signals.

The common feature of all the possibilities for defining the control signals W1A and W1B such that they can or cannot be changed is that these control signals can be matched to the actual circumstances simply, that is to say at least without extensively redesigning the clock generator and/or the circuit, even after production of the clock generator and/or of the circuit to be driven by it. This matching can be optimal in each case, and not merely approximate. As already mentioned in the introduction, this is particularly advantageous for clock signal generators which are integrated in integrated circuits.

Although, in the exemplary embodiment under consideration, the control signals W1A and W1B can be used to influence the change in the duty ratio of the input clock signal CLK both with regard to type (control signal W1A) and with regard to extent (control signal W1B), there is no restriction on the provision of this (recurring) possibility for exerting an influence. This means that, if need be, one and/or other of these possibilities (omitting or including the corresponding circuit components) may be sacrificed.

The influence on the duty ratio which may be exerted using the control signals W1A and W1B enables, on its own or in conjunction with the ability to set the duration of the overlap-free phase, which is yet to be explained, extremely precise individual matching to the particular circumstances.

The second block **200** will now be explained in greater detail with reference to FIG. **3**.

The second block **200** can be subdivided into two sub-blocks of largely identical design, namely a first sub-block for generating the first output clock signal PHI1, and a second sub-block for generating the second output clock signal PHI2.

The first sub-block comprises an AND gate **210**, an OR gate **220**, a transistor pair **230** (in this case, a pair of field-effect transistors) driven by the AND gate and the OR gate, and a delay stage **240**, which are wired up as shown in FIG. **3**.

The core element of the first sub-block in the circuit shown in FIG. **3** is the delay stage **240**.

If this delay stage **240** were to be replaced by a continuous conduction element, the output signal PHI1 output from the first sub-block of the second block **200** would correspond exactly to the inverted input signal (intermediate clock signal) CLK1. This is because the transistor associated with the AND gate **210** outputs a low level when the output of the AND gate is at high level ("1"), and the transistor associated with the OR gate **220** outputs a high level when the output of the OR gate **220** is at low level ("0").

In contrast to this, as a result of the delay stage **240** being provided, the OR gate **220** can receive the input signal received from the delay stage offset in time such that the time of the high-level phase of the output signal from the OR

gate is lengthened (this phase cannot be shortened because the second input signal of the OR gate **220** is the input signal CLK1 itself, which is input into the second block **200**, and the minimum duration of the high-level phase of the output signal from the OR gate thus cannot be changed, i.e., it is defined such that it cannot be changed by the delay stage **240**), with the result that the time for which the transistor associated with the OR gate is switched on, and therefore also the time for which the high-level voltage is switched through to the output PHI1, is noticeably shortened. Ultimately, providing the delay stage **240** in the first sub-block of the second block **200** thus causes the first output clock signal PHI1 to be influenced such that—in comparison with the case where no signal delay is provided—it rises to the high level later or drops to the low level sooner than is the case with the input signal CLK1.

The design of the second sub-block of the second block **200** is identical to that of the first sub-block. That is to say, the second sub-block has an AND gate **260** corresponding to the AND gate **210**, an OR gate **270** corresponding to the OR gate **220**, a transistor pair **280** corresponding to the transistor pair **230**, and a delay stage **290** corresponding to the delay stage **240**, which are wired up as shown in FIG. **3**.

In contrast to the first sub-block, the signal input into the second sub-block is the inverted version of the signal CLK1 input into the first sub-block, i.e. CLK1, this version having been inverted by means of an invertor. Furthermore, the signals which are to be delayed by the delay stages **240** and **290** are different (PHI2 in the case of delay stage **240** in the first sub-block; PHI1 in the case of delay stage **290** in the second sub-block).

These differences do not change anything about the fundamental functional and operational correspondence between the first and the second sub-block, however.

As in the case of the first sub-block, the core element of the second sub-block in the circuit shown in FIG. **3** is also the delay stage **290**.

If this delay stage **290** were to be replaced by a continuous conduction element, the output signal PHI2 output from the second sub-block of the second block **200** would correspond exactly to the inverse of the input signal CLK1, i.e. exactly to CLK1. This is because the transistor associated with the AND gate **260** outputs a low level when the output of the AND gate is at high level ("1"), and the transistor associated with the OR gate **270** outputs a high level when the output of the OR gate is at low level ("0").

In contrast to this, as a result of the delay stage **290** being provided, the OR gate **270** can receive the input signal received from said delay stage offset in time such that the time of the high-level phase of the output signal from the OR gate is lengthened (this phase cannot be shortened because the second input signal of the OR gate **270** is the signal CLK1 itself, which is input into the second sub-block, and the minimum duration of the high-level phase of the output signal from the OR gate thus it cannot be changed, more precisely is defined such that it cannot be changed by the delay stage **290**), with the result that the time for which the transistor associated with the OR gate **270** is switched on, and therefore also the time for which the high-level voltage is switched through to the output PHI2, is noticeably shortened. Ultimately, providing the delay stage **290** in the second sub-block of the second block **200** thus causes the second output clock signal PHI2 to be influenced such that—in comparison with the case where no signal delay is provided—it rises to the high level later or drops to the low level sooner than is the case with the input signal CLK1.

Shortening the high-level phases (lengthening the low-level phases) of the output clock signals PHI1 and/or PHI2, whose waveforms are naturally inverse or complementary, that is to say without any delay stages, automatically causes a so-called overlap-free phase to be provided which did not exist initially and in which both the output clock signal PHI1 and the output clock signal PHI2 are in a low-level phase.

The circuit is preferably designed in such a way that a capacitor situated at the outputs PHI1/PHI2 automatically increases the overlap-free time, and the overlap-free times of the delay stages **240/290** may be combined with this cumulatively.

The extent to which the high-level phases of the output clock signals PHI1 and/or PHI2 are shortened (the low-level phases are lengthened) and the duration of the overlap-free phase obtained as a result are determined by the extent of the delay(s) by the delay stages **240** and/or **290**. These delay stages are thus designed, according to the invention, such that they each have a multiplicity of delay elements **241** to **244** or **291** to **294**, which are wired up in parallel, and a selection device in the form of a multiplexer **245** or **295**. The plurality of delay elements **241** to **244** or **291** to **294** are designed in such a manner that they can be used to produce delays, for the signals input in each case, which can be defined as required but which are different from one another; in so doing, it may also be permitted in each case for a delay to be equal to zero, that is to say for there to be no delay. All the delay elements of a particular delay stage receive one and the same input signal, namely the signal PHI2 (delay elements of delay stage **240**) or PHI1 (delay elements of delay stage **290**). The signals input in each case are delayed by the respective delay element according to the respective delay, but are output otherwise unchanged as the respective output signal. The output signals from all delay elements **241** to **244** and **291** to **294** are input into the respective multiplexers **245** and **295**. The multiplexers **245** and **295** can be used to select or determine, as a function of the control signals W2A and W2B supplied to them externally, which of the signals input into the respective multiplexers **245** and **295** is to be output as the output signal of the latter.

The control signals W2A and W2B input externally into the second block **200** or into its multiplexers **245** and **295** thus enable the duration of the overlap-free phase of the output clock signals PHI1 and PHI2 to be set or purposefully changed. They therefore permit, on their own or in conjunction with the duty ratio setting undertaken in the first block **100**, the output clock signals PHI1 and PHI2 to be matched to the particular circumstances selectively, individually and in each case optimally.

As regards storage or other defining of the control signals W2A and W2B, more precisely their waveforms and/or values, reference is made to the corresponding statements about the control signals W1A and W1B.

The number of delay elements to be provided per delay stage can be defined as desired both in the first block and in the second block independently of one another. The extent of the delay, which is produced by the respective delay elements, can also be defined individually. In particular, as mentioned above, it is also possible to provide a "delay element" with the delay zero in each case.

It is naturally also possible to omit individual components of the clock generator described. The components to be omitted may be a whole block as shown in FIG. **1**, or alternatively "only" selected individual or numbers of multiplexers, including any signal paths which are then superfluous, as shown in FIGS. **2** and/or **3**.

In the exemplary embodiment described, it has been assumed that the rising edges or the high-level phases of the respective output clock signals are the events or phases which trigger an event in the equipment to be driven by these signals. Instead of this, it is naturally also possible for the falling edges or the low-level phases of the respective output clock signals to be the events or phases which trigger an event in the equipment to be driven by these signals; the circuit described then needs to be modified accordingly, particularly as regards setting the overlap-free phase in the second block **200**. Those skilled in the art are quite enabled to implement such a modification without any detailed explanation.

We claim:

1. A clock signal generator, comprising:

a clock input;

a first logic configuration having an input receiving an intermediate clock signal and outputting a first clock output signal;

a second logic configuration having an input receiving the intermediate clock signal and outputting a second clock output signal;

the first and second clock output signals having a programmable duty ratio and a programmable overlap-free time;

a first delay stage with a selectable delay connected to receive the second clock output signal and to supply the second clock output signal to said first logic configuration;

a second delay stage with a selectable delay connected to receive the first clock output signal and to supply the first clock output signal to said second logic configuration;

a third delay stage with a selectable delay, said third delay stage having an input connected to said clock input; and

a third logic configuration having an input connected to said clock input and outputting the intermediate clock signal to said input of said first logic configuration and to said input of said second logic configuration.

2. The clock signal generator according to claim **1**, which further comprises a multiplexer for selecting a delayed signal, said multiplexer being connected to a multiplicity of mutually parallel delay paths and being controllable by an external control signal.

3. The clock signal generator according to claim **1**, which further comprises a multiplicity of mutually parallel delay paths, and wherein a delayed signal is selectable by modifying a wiring of said multiplicity of delay paths.

4. The clock signal generator according to claim **1**, further comprises a circuit with a multiplicity of mutually parallel delay paths, and wherein a delayed signal is selectable by subsequently breaking wiring connections in said circuit with said multiplicity of delay paths.

5. The clock signal generator according to claim 4, wherein said wiring connections are broken by means of a laser beam.

6. The clock signal generator according to claim **1**, wherein said third logic circuit has an AND gate and an OR gate each having a first input receiving the clock input signal and a second input receiving the signal delayed in said third delay stage, and wherein the intermediate clock signal is selectively tapped off at an output of said AND gate and an output of said OR gate.

* * * * *

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McCracken et al.

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(45) **Date of Patent: Aug. 21, 2001**

(54) **CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY**

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(73) Assignee: **Silicon Graphics, Inc.**, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Sep. 30, 1999**

(51) **Int. Cl.**[7] **G06F 12/00**
(52) **U.S. Cl.** **711/105**
(58) **Field of Search** 711/105, 104, 711/101; 365/193, 194

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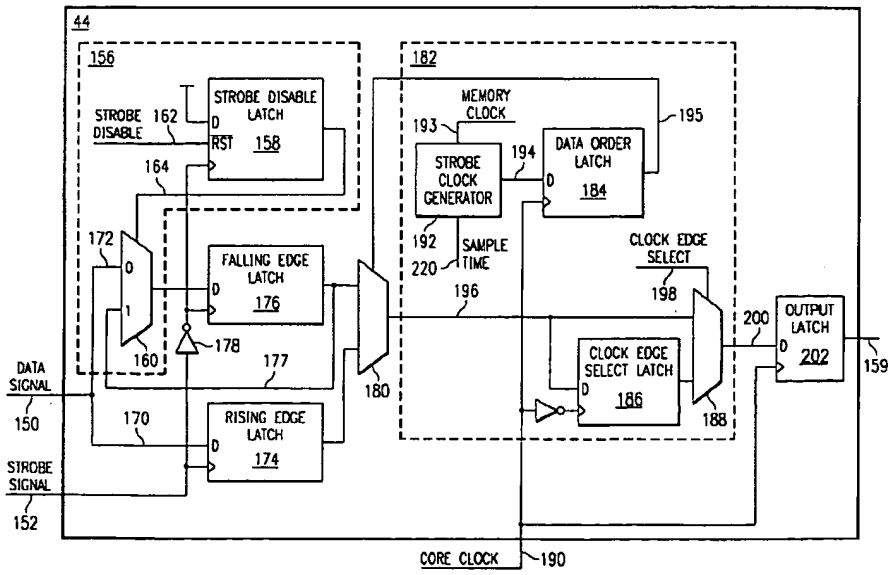
Primary Examiner—Tuan V. Thai
Assistant Examiner—Stephen C. Elmore
(74) *Attorney, Agent, or Firm*—Baker Botts L.L.P.

(57) **ABSTRACT**

A configurable synchronizer (**10**) for DDR-SDRAM (**12**) is provided that includes a strobe select module (**40**) operable to receive a memory select signal (**106**) and to pass strobe signals (**20, 30**) from one or more DDR-SDRAMs (**16, 18**) to a number of synchronizer circuits (**44**) corresponding to data signals (**17**) passed in parallel by each DDR-SDRAM as indicated by the memory select signal (**106**). A rising edge latch (**174**) receives a rising edge data signal (**170**) and latches the rising edge data signal (**170**) through the rising edge latch (**174**) on a rising edge of the strobe signal (**152**). A falling edge latch (**176**) receives a falling edge data signal (**172**) and latches the falling edge data signal (**172**) through the falling edge latch (**176**) on a falling edge of the strobe signal (**152**). A data signal selector (**180**) receives a data order control signal (**195**) and forwards the rising edge data signal (**170**) from the rising edge latch (**174**) to an intermediate output (**196**) on either a rising edge of a memory clock cycle (**193**) or a falling edge of a memory clock cycle (**193**) followed by forwarding the falling edge data signal (**172**) from the falling edge latch (**176**) to the intermediate output (**196**) on an opposite edge of the memory clock cycle (**193**) in response to the data order control signal (**195**). An output latch (**202**) receives the intermediate output (**196**) and latches the intermediate output (**196**) through the output latch (**202**) to an output signal (**154**) on each core clock cycle (**190**).

20 Claims, 4 Drawing Sheets



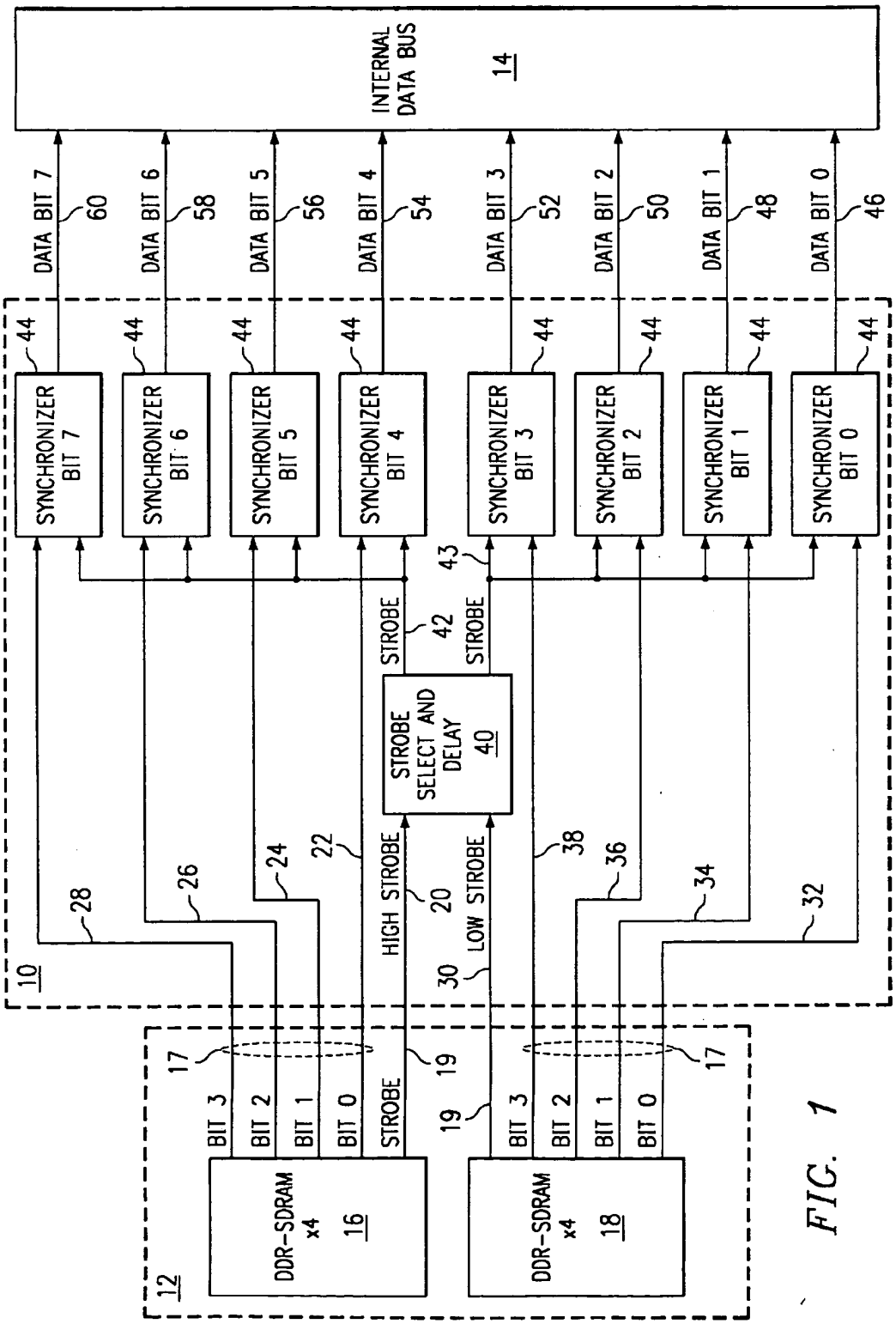

INTERNAL DATA BUS
14
DATA BIT 7
60
DATA BIT 6
58
DATA BIT 5
56
DATA BIT 4
54
DATA BIT 3
52
DATA BIT 2
50
DATA BIT 1
48
DATA BIT 0
46
SYNCHRONIZER BIT 7
SYNCHRONIZER BIT 6
SYNCHRONIZER BIT 5
SYNCHRONIZER BIT 4
SYNCHRONIZER BIT 3
SYNCHRONIZER BIT 2
SYNCHRONIZER BIT 1
SYNCHRONIZER BIT 0
44
43
STROBE
42
STROBE SELECT AND DELAY
40
HIGH STROBE
20
LOW STROBE
30
22
24
26
28
32
34
36
38
10
17
19
BIT 3
BIT 2
BIT 1
BIT 0
STROBE
DDR-SDRAM x4
16
18
12

FIG. 1

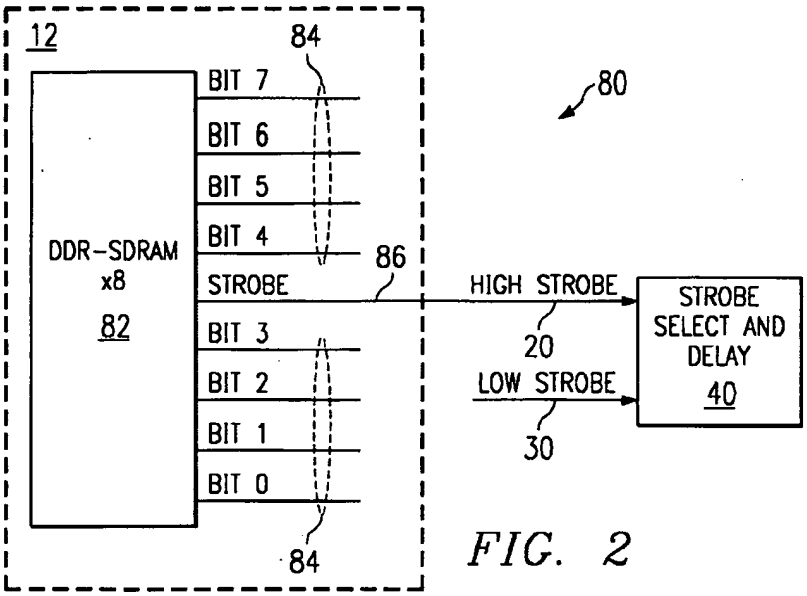

12
84
BIT 7
BIT 6
BIT 5
BIT 4
DDR-SDRAM
x8
82
STROBE
86
BIT 3
BIT 2
BIT 1
BIT 0
84
80
HIGH STROBE
20
LOW STROBE
30
STROBE
SELECT AND
DELAY
40

FIG. 2

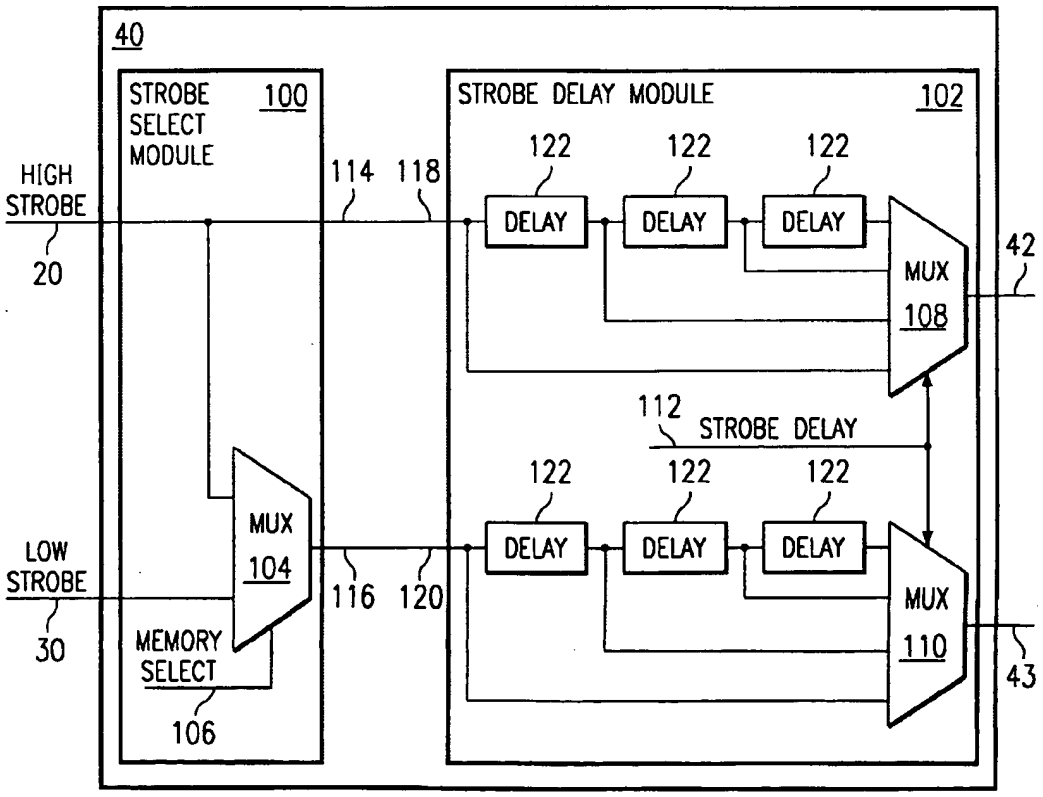

40
STROBE
SELECT
MODULE
100
STROBE DELAY MODULE
102
HIGH
STROBE
20
114
118
122
122
122
DELAY
DELAY
DELAY
MUX
108
42
112
STROBE DELAY
LOW
STROBE
30
MUX
104
116
120
MUX
110
43
MEMORY
SELECT
106

FIG. 3

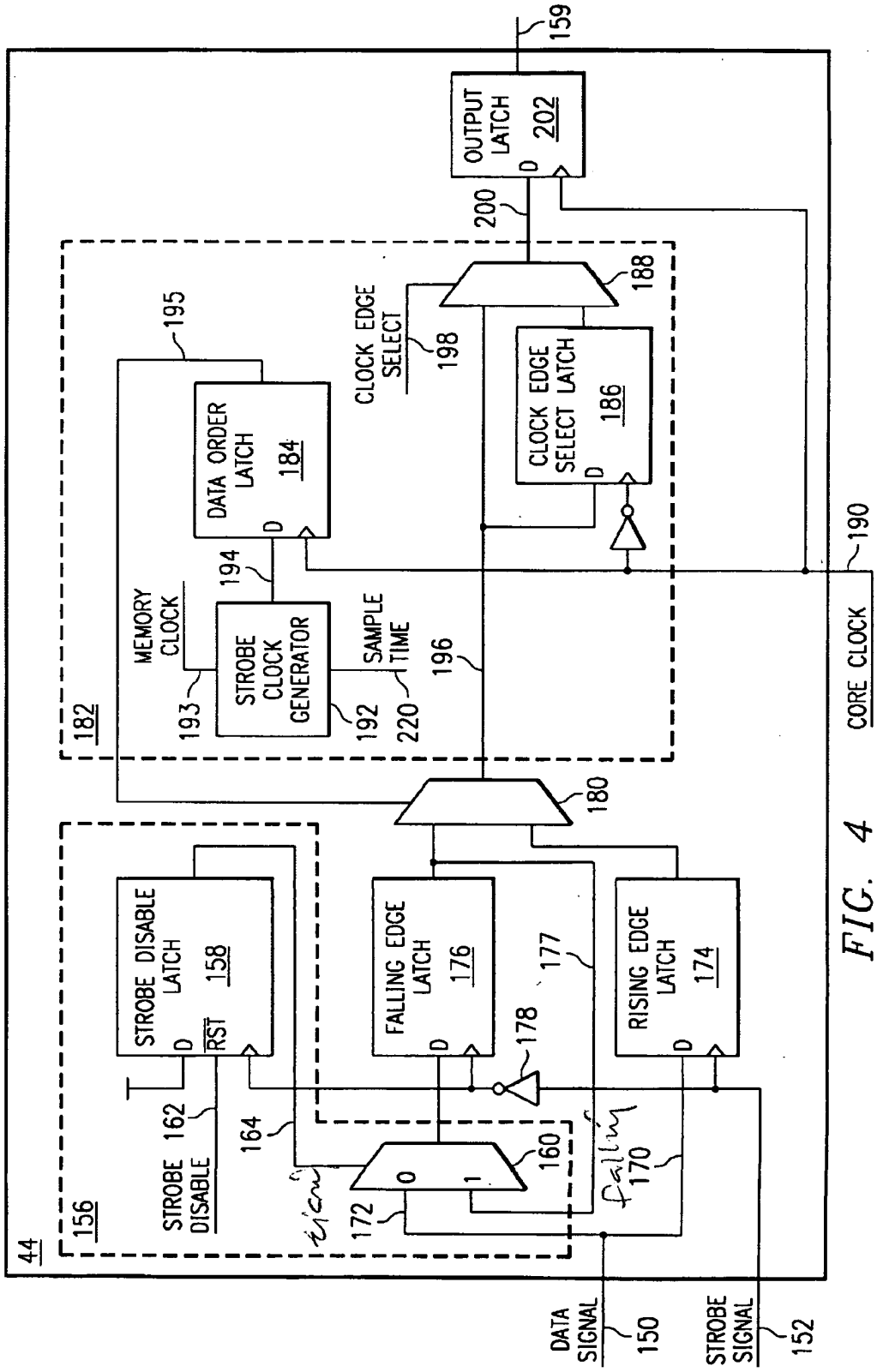

159
OUTPUT LATCH 202
200
188
CLOCK EDGE SELECT
198
CLOCK EDGE SELECT LATCH 186
195
DATA ORDER LATCH 184
194
MEMORY CLOCK
193
STROBE CLOCK GENERATOR
192
SAMPLE TIME
220
196
182
190
CORE CLOCK
180
STROBE DISABLE LATCH 158
RST
FALLING EDGE LATCH 176
177
178
RISING EDGE LATCH 174
162
STROBE DISABLE
164
160
172
170
156
44
DATA SIGNAL 150
STROBE SIGNAL 152

FIG. 4

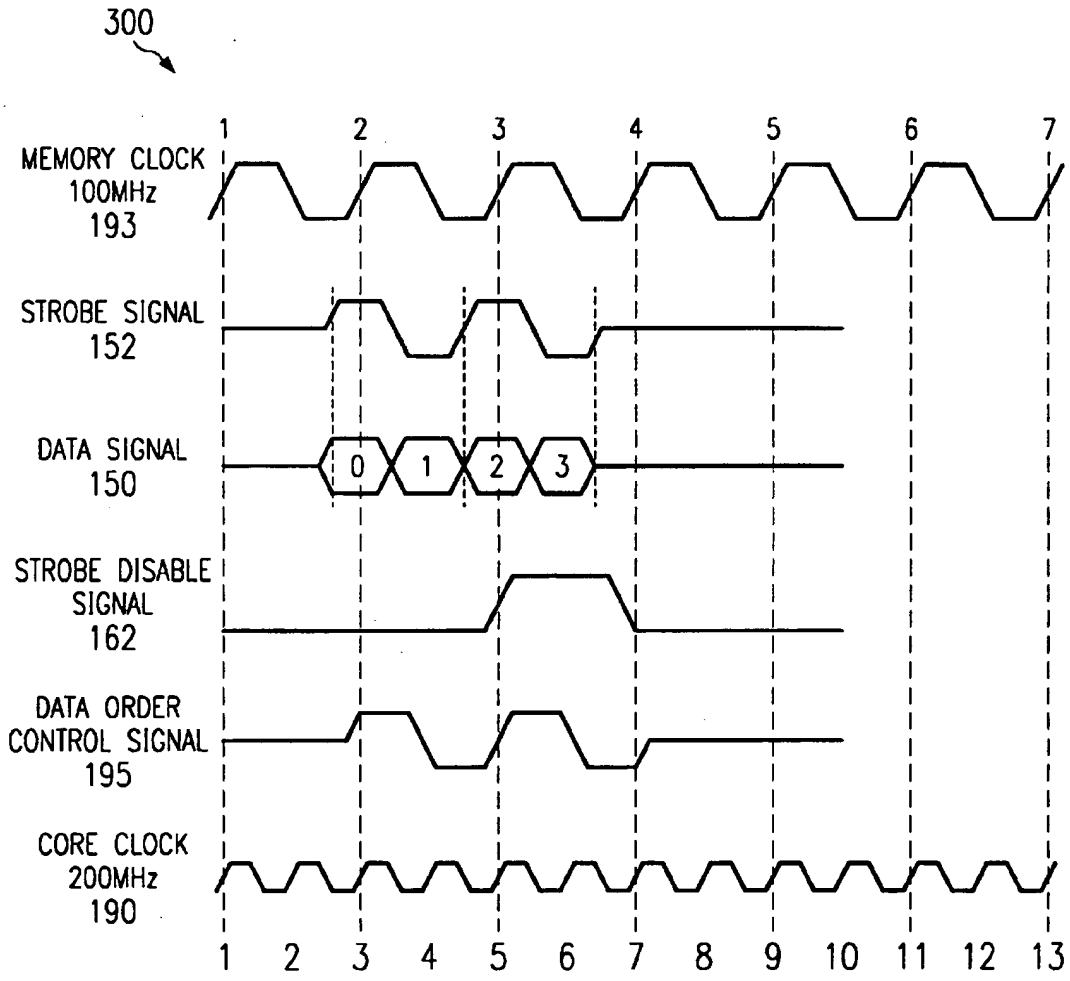

300
MEMORY CLOCK
100MHz
193
STROBE SIGNAL
152
DATA SIGNAL
150
STROBE DISABLE
SIGNAL
162
DATA ORDER
CONTROL SIGNAL
195
CORE CLOCK
200MHz
190
0
1
2
3
1 2 3 4 5 6 7
1 2 3 4 5 6 7 8 9 10 11 12 13

FIG. 5

CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of computer systems and more particularly to an improved configurable synchronizer for double data rate synchronous dynamic random access memory (DDR-SDRAM).

BACKGROUND OF THE INVENTION

A computer system is generally comprised of several component parts including a processor, random access memory, a data bus, and other peripheral devices and components. The processor accesses, modifies, and writes data to random access memory. The data contained in random access memory is transferred to the processor through the data bus. One type of random access memory is dynamic random access memory (DRAM). As computer processor speeds increase, faster random access memory is needed to fully realize the potential of faster processor chips. One solution for faster random access memory is synchronous DRAM (SDRAM). SDRAM is tied to a system clock and is designed to be able to read or write from memory in burst mode (after the initial read or write latency) at one clock cycle per access (zero wait states) at memory bus speeds up to 100 MHz. However, current computer processor speeds often exceed the capability of SDRAM to provide data from memory.

Double Data Rate Synchronous Dynamic Random Access Memory (DDR-SDRAM) addresses the need for faster random access memory. DDR-SDRAM is similar in function to regular SDRAM, but it doubles the bandwidth of the memory by transferring data twice per cycle, on both the rising and falling edges of the clock signal. DDR-SDRAM returns a strobe signal synchronously with data signals. The strobe signal is related to the memory clock signal and indicates when valid data is ready for transfer from the DDR-SDRAM. Data signals are available on both the rising edge of the strobe signal and the falling edge of the strobe signal. Thus, two data signals are available with each clock cycle of a memory clock used for the DDR-SDRAM. In order to use DDR-SDRAM, the computer processor needs to synchronize the data coming from the DDR-SDRAM with the internal core clock of the computer processor chip. The internal core clock is often used to clock the data bus across which the data signals from the DDR-SDRAM are sent to the computer processor chip.

DDR-SDRAM may use a variety of DRAM configurations such as 4-bit DRAMs, 8-bit DRAMs, 16-bit DRAMs, or 32-bit DRAMs. Conventional synchronizers for DDR-SDRAM are usually designed for a single DDR-SDRAM configuration. Due to variations in DDR-SDRAM, the computer processor chip, and mother boards, strobe signals and data signals may not arrive together at the synchronizer. Conventional synchronizers for DDR-SDRAM are usually designed for a particular situation where the strobe signal and data signals do not arrive together. Therefore, it is desirable to provide a configurable synchronizer for DDR-SDRAM that allows the synchronizer to be optimized for various implementations.

SUMMARY OF THE INVENTION

From the foregoing, it may be appreciated that a need has arisen for a configurable synchronizer for DDR-SDRAM that provides improved flexibility and configurability. In accordance with the present invention, a configurable synchronizer for DDR-SDRAM is provided that substantially eliminates and reduces disadvantages and problems associated with conventional memory synchronizers.

According to an embodiment of the present invention, a configurable synchronizer for DDR-SDRAM is provided that includes a strobe select module operable to receive a memory select signal and to pass strobe signals from one or more DDR-SDRAMs to a number of synchronizer circuits corresponding to data signals passed in parallel by each DDR-SDRAM as indicated by the memory select signal. Each synchronizer circuit includes a rising edge latch for receiving a rising edge data signal from the DDR-SDRAM and to latch the rising edge data signal through the rising edge latch on a rising edge of the strobe signal. Each synchronizer circuit further includes a falling edge latch for receiving a falling edge data signal from the DDR-SDRAM and to latch the falling edge data signal through the falling edge latch on a falling edge of the strobe signal. Each synchronizer circuit further includes a data signal selector for receiving a data order control signal and to forward the rising edge data signal from the rising edge latch to an intermediate output on either a rising edge of a memory clock cycle or a falling edge of a memory clock cycle followed by forwarding the falling edge data signal from the falling edge latch to the intermediate output on an opposite edge of the memory clock cycle in response to the data order control signal. Each synchronizer circuit further includes an output latch operable to receive the intermediate output and to latch the intermediate output through the output latch to an output signal on each core clock cycle.

The present invention provides various technical advantages over conventional memory synchronizers. For example, one technical advantage is allowing various DDR-SDRAM configurations to be used with the configurable synchronizer. Another technical advantage is to provide several delay periods to delay a strobe signal so that it arrives with its associated data signals. Yet another technical advantage is to prevent false data signals from entering the configurable synchronizer by disabling the strobe signal after the last data signal is captured by the configurable synchronizer. A further technical advantage is in synchronization between the strobe signals and data signals from the DDR-SDRAM and a data bus clocked by an internal core clock with the synchronization window being movable in quarter cycle increments of a memory clock. Other technical advantages may be readily apparent to one skilled in the art from the following figures, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numbers represent like parts and wherein:

FIG. **1** is a block diagram of DDR-SDRAM coupled to data bus through a memory synchronizer;

FIG. **2** illustrates the DDR-SDRAM of FIG. **1** as an 8 bit DDR-SDRAM;

FIG. **3** illustrates a strobe select module and a strobe delay module;

FIG. **4** illustrate a synchronizer circuit for a data bit; and

FIG. **5** illustrates a timing diagram for the memory synchronizer.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**, a configurable synchronizer for communications between DDR-SDRAM and an internal

data bus is generally indicated at **10**. In one embodiment, configurable synchronizer **10** synchronizes eight bits of DDR-SDRAM with an internal data bus **14**. However, configurable synchronizer **10** may synchronize any suitable number of DDR-SDRAM bits with internal data bus **14**. A block of DDR-SDRAM **12** provides input to configurable synchronizer **10** and may include eight bits of DDR-SDRAM corresponding to the eight data bits synchronized with internal data bus **14** by configurable synchronizer **10**. It should be noted that internal data bus **14** may have a bandwidth of sixteen bits, thirty-two bits or more. However, any suitable data bus size may be used. Thus, for purposes of this disclosure, eight bits of data are transferred in parallel from block of DDR-SDRAM **12** through configurable synchronizer **10** into internal data bus **14**. Additional configurable synchronizers **10** and blocks of DDR-SDRAM **12** may be used to provide internal data bus **14** with a number of data bits corresponding to the bandwidth of internal data bus **14**. In one embodiment, a memory clock controls the operating frequency of block DDR-SDRAM **12** and core clock controls the operating frequency of internal data bus **14**. In that embodiment, the memory clock operates at one-half the operating frequency of the core clock. For example, if the core clock operates at 200 megahertz, the memory clock would operate at 100 megahertz.

Various configurations of DDR-SDRAM may be used including 4-bit, 8-bit, or 16-bit configurations. In one embodiment, block of DDR-SDRAM **12** includes a high 4-bit DDR-SDRAM **16** and a low 4-bit DDR-SDRAM **18**. Each 4-bit DDR-SDRAM has a strobe signal **19** and an output line **17** for each bit stored in the DDR-SDRAM. The strobe signal **19** indicates when valid data is available on the output lines **17**. Strobe signal **19** is related to a memory clock signal used to clock block of DDR-SDRAM **12**.

Configurable synchronizer **10** has inputs for eight bits numbered from bit **0** in the low order position to bit **7** in the high order position. These inputs include a bit **0** input **32**, a bit **1** input **34**, a bit **2** input **36**, a bit **3** input **38**, a bit **4** input **22**, a bit **5** input **24**, a bit **6** input **26**, and a bit **7** input **28**. Configurable synchronizer **10** also includes two strobe signal inputs so that configurable synchronizer **10** may process variously configured blocks of DDR-SDRAM **12** consisting of different subject DDR-SDRAMs. The two strobe signals are a high strobe input **20** and a low strobe input **30**. Configurable synchronizer **10** also includes an output for each data bit input. The outputs include a bit **0** output **46**, a bit 1 output **48**, a bit **2** output **50**, a bit **3** output **52**, a bit **4** output **54**, a bit **5** output **56**, a bit **6** output **58**, and a bit **7** output **60**. The outputs of configurable synchronizer **10** are coupled to inputs for internal data bus **14**.

In the embodiment of block of DDR-SDRAM **12** illustrated in FIG. **1** where block of DDR-SDRAM **12** includes high 4-bit DDR-SDRAM **16** and low 4-bit DDR-SDRAM **18**, the strobe signal **19** from high 4-bit DDR-SDRAM **16** is coupled to high strobe input **20** of configurable synchronizer **10**. The output lines **17** of high 4-bit DDR-SDRAM **16** are coupled as follows to configurable synchronizer **10**: bit **0** output line **17** is coupled to bit **4** input **22**; bit **1** output line **17** is coupled to bit **5** input **24**; bit **2** output line **17** is coupled to bit **6** input **26**; and bit **3** output line **17** is coupled to bit **7** input **28**. The strobe signal **19** for low 4-bit DDR-SDRAM **18** is coupled to low strobe input **30**. The output lines for low 4-bit DDR-SDRAM **18** are coupled as follows to configurable synchronizer **10**: bit **0** output line **17** is coupled to bit **0** input **32**; bit **1** output line **17** is coupled to bit **1** input **34**; bit **2** output line **17** is coupled to bit **2** input **36**; and bit **3** output line **17** is coupled to bit **3** input **38**.

High strobe input **20** and low strobe input **30** are coupled to a strobe select and delay module **40**. Strobe select and delay module **40** provides strobe control signals for a plurality of synchronizer circuits **44**. Strobe select and delay module **40** may provide two sets of strobe control signals, high strobe control signals **42** and low strobe control signals **43**, so that block of DDR-SDRAM **12** may use various configurations of DDR-SDRAM. Since block of DDR-SDRAM may use two 4-bit DDR-SDRAMs, synchronizer circuits **44** are grouped in two sets of four synchronizer circuits **44** so that a common control signal may be sent to each synchronizer circuit **44** in the group processing a parallel set of four data bits from a 4-bit DDR-SDRAM. The number of synchronizer circuits **44** corresponds to the number of data bit inputs and data bit outputs for configurable synchronizer **10**. Thus, each data bit input line is coupled to a synchronizer circuit **44**, and each data bit output line is also coupled to an output of a corresponding synchronizer circuit **44**. Synchronizer circuits **44** synchronize data received from a common bank of DDR-SDRAM using a common strobe signal since data is available in parallel on the output lines of the common of DDR-SDRAM. Each synchronizer circuit **44** synchronizes a data bit of DDR-SDRAM **12** with internal data bus **14**.

Referring to FIG. **2**, an embodiment of block of DDR-SDRAM **12** using an 8-bit DDR-SDRAM is generally indicated at **80**. Block of DDR-SDRAM **12** includes an 8-bit DDR-SDRAM **82**. 8-bit DDR-SDRAM **82** includes eight output lines **84** corresponding to each data bit transferred in parallel by 8-bit DDR-SDRAM **82** and a strobe signal **86** to indicate when valid data is available on the eight output lines **84**. The eight output lines **84** of 8-bit DDR-SDRAM **82** are coupled to the eight corresponding data bit inputs of configurable synchronizer **10**. The strobe signal **84** is coupled to high strobe input **20**. Low strobe input **30** has no input. Strobe select and delay module **40** knows that block of DDR-SDRAM **80** consists of a single 8-bit DDR-SDRAM **82** and provides the same strobe control signals to each synchronizer circuit **44** in configurable synchronizer **10**. Thus, strobe select and delay module **40** forwards the same strobe control signals across high strobe control signal **42** and low strobe control signal **43**.

Referring to FIG. **3**, strobe select and delay module **40** is illustrated. Strobe select and delay module **40** includes a strobe select module **100** and a strobe delay module **102**. Strobe select module **100** includes a multiplexor **104** and a memory select signal **106**. High strobe input **20** and low strobe input **30** provide inputs to multiplexor **104**, and memory select signal **106** provides a control signal for multiplexor **104**. Memory select signal **106** indicates a bit size for DDR-SDRAM modules in block of DDR-SDRAM **12** currently being processed by configurable synchronizer **10**. Memory select signal **106** may indicate that block of DDR-SDRAM **12** uses either 4-bit or 8-bit DDR-SDRAM modules. Memory select signal **106** is dynamic and may change as different blocks of DDR-SDRAM **12** are processed by configurable synchronizer **10**. If memory select signal **106** indicates 4-bit DDR-SDRAM modules, high strobe input **20** and low strobe input **30** both receive valid strobe signals and are passed directly to high strobe output **114** and low strobe output **116**, respectively. If memory select signal **106** indicates that an 8-bit DDR-SDRAM module is coupled to strobe select module **40**, high strobe input **20** receives a valid strobe signal, but low strobe input **30** has no input. In that case, multiplexor **104** forwards high strobe input **20** to low strobe output **116** so that both high strobe output **114** and low strobe output **116** are identical.

This ensures that high strobe control signal **42** and low strobe control signal **43** are identical and correspond to the single strobe signal **86** of the 8-bit DDR-SDRAM **82**.

Strobe delay module **102** receives high strobe output **114** on a high strobe delay input **118** and low strobe output **116** on a high strobe delay input **120**. Strobe delay module **102** delays high strobe delay input **118** and low strobe delay input **120** as indicated by a strobe delay signal **112** before forwarding high strobe delay input **118** to high strobe control signal **42** and low strobe delay input **120** to low strobe control signal **43**.

Strobe delay signal **112** provides a control signal for both a high multiplexor **108** and a low multiplexor **110**. In one embodiment, strobe delay signal **112** may indicate one of four delays: 0 nanoseconds; 0.9 nanoseconds; 1.8 nanoseconds; or 2.7 nanoseconds. Both high strobe delay input **118** and low strobe delay input **120** are delayed by the same amount of time. Although the present embodiment provides four different delay periods, any number of delay periods of any suitable length may be used. In the present embodiment, three standard delays **122** are coupled in series between high strobe delay **118** and high multiplexer **108**. Each delay **122** provides approximately 0.9 nanoseconds of delay. An input to each delay **122** is coupled to high multiplexer **108** thereby providing high strobe delay input **118** to high multiplexer **108** at each of four delay periods as previously described. Similarly, three standard delays **122** are coupled in a series between low strobe delay **120** and low multiplexer **110**. Strobe delay signal **112** determines which delayed signal will be forwarded to high strobe control signal **42** and low strobe control signal **43**. Strobe delay module **102** provides flexibility and configurability to account for differences in arrival time between strobe signals **19** and data signals **17** at configurable synchronizer **10**. Strobe delay module **102** allows strobe signals from block of DDR-SDRAM **12** to be delayed such that the strobe signals are within the center of a data valid window. The data valid window of time during which data signals from block of DDR-SDRAM **12** are valid at synchronizer circuit **44**. Strobe delay signal **112** is a static signal set during system testing to optimize performance of configurable synchronizer **10**. Once strobe delay signal **112** is set, it generally is not changed unless system components change.

Referring to FIG. **4**, a synchronizer circuit **44** is illustrated. Synchronizer circuit **44** receives a data signal **150** from block of DDR-SDRAM **12** and a strobe signal **152** from strobe select and delay module **40**. Synchronizer circuit **44** generates an output signal **154**. DDR-SDRAM can provide data signals on both the rising edge and the falling edge of a memory clock signal. Therefore, DDR-SDRAM may transfer two bits of data across the same line in one memory clock cycle. Strobe signal **152** is related to a memory clock cycle signal. Strobe signal **152** is present when data is available at data signal **150**. Strobe signal **152** has a period equal to the memory clock cycle. However, the rising and falling edges of strobe signal **152** may be slightly offset from the rising and falling edges of the memory clock cycle due to circuit path lengths and other factors.

Since DDR-SDRAM can provide data signals on both the rising edge and falling edge of strobe signal **152**, data signal **150** is split into a rising edge data signal **170** and a falling edge data signal **172**. Rising edge data signal **170** is coupled to a rising edge latch **174**, and falling edge data signal **172** is coupled through a strobe disable multiplexer **160** to a falling edge latch **176**.

Strobe signal **152** is coupled to the clock inputs of rising edge latch **174** and falling edge latch **176**. Rising edge latch **174** may be a D-type flip-flop and may change states with each rising edge of strobe signal **152**. An inverter **178** inverts strobe signal **152** causing falling edge latch **176** to change state on the falling edge of strobe signal **152**. Therefore, on the rising edge of strobe signal **152**, a data value from rising edge data signal **170** is latched into rising edge latch **174**, and on the falling edge of strobe signal **152**, a data value from falling edge data signal **172** is latched into falling edge latch **176**.

Since data signals **150** may be provided on both the rising edge and the falling edge of strobe signal **152** and strobe signal **152** is bi-directional, false data may be processed in configuration synchronizer **10** after the last falling edge of strobe signal **152** during a read burst. Depending on the termination scheme of strobe signal **152**, strobe signal **152** may be either a logic level 1 or a logic level 0 after the last falling edge of the read burst. If the last falling edge of the read burst happens before the end of the core clock cycle, the block of DRR-SDRAM **12** may release the data bus **14** thereby causing invalid data to be latched into falling edge latch **176** overwriting valid data that has not yet been latched out of falling edge latch **176** towards output latch **202**. A strobe disable section **156** of synchronizer circuit **44** prevents invalid data from being latched into falling edge latch **176** after the last falling edge of strobe signal **152** related a read burst.

Strobe disable section **156** includes a strobe disable latch **158**, a strobe disable multiplexer **160**, and a strobe disable signal **162**. Strobe disable section **156** may also be referred to as a strobe disable module. Strobe disable latch **158** includes an input line with a constant logic level "1" signal, a reset line operable when its input is a logic level "0", and an output line. Strobe disable signal **162** is coupled to the reset line, and the output line provides a control signal for strobe disable multiplexer **160**. Strobe disable latch **158** is clocked by an inversion of strobe signal **152**. Thus, strobe disable latch **158** changes state on the falling edge of strobe signal **152**.

Strobe disable latch **158** provides a control signal **164** for strobe disable multiplexer **160**. A control signal **164** of logic level "0" causes strobe disable multiplexer **160** to forward falling edge data signal **172** to falling edge latch **176** and to the remainder of synchronizer circuit **44**. A control signal **164** of logic level "1" causes the output of falling edge latch **176** to recirculate through strobe disable multiplexer **160** using a recirculate path **177** thereby preventing a change in state of falling edge latch **176** until strobe disable signal **162** enables strobe disable latch **158**.

Strobe disable signal **162** is a dynamic control signal that indicates when valid data is available for processing on data signal **150**. When valid data is available, the strobe disable signal **162** is a logic level "0" thereby causing strobe disable latch **158** to reset and provide a control signal **164** of logic level "0". After the last falling edge of strobe signal **152** related to a read burst, strobe disable signal **162** indicates that the final data value of the read burst has been obtained and that no further data values are currently available. After the final data value, strobe disable signal **162** is a logic level "1" causing strobe disable latch **158** to latch the "D" input (logic level "1") through to control signal **164**.

A data order multiplexer **180** alternately forwards the output of rising edge latch **174** and the output of falling edge latch **176** to a configuration section **182** of synchronizer circuit **44**. Configuration section **182** allows for quarter cycle granularity with respect to synchronizing block of DDR-SDRAM **12** with internal data bus **14**. Configuration section **182** includes s strobe clock generator **192**, a data order latch **184**, a clock edge select latch **186**, and a clock edge select multiplexer **188**. A core clock **190** provides clock input for data order latch **184** and clock edge select latch **186**.

A strobe clock generator **192** generates a strobe clock signal **194** for controlling the operation of data order mul-

tiplexer **180**. Strobe clock generator **192** receives a sample time **220** and a memory clock **193** and generates a strobe clock signal **194**. Strobe clock signal **194** is latched through data order latch **184** to provide a data order control signal **195** to data order multiplexer **180**. Memory clock **193** generates a clock signal with each clock cycle having a rising edge and a falling edge. Strobe clock generator **192** alternates strobe clock signal **194** with each edge of memory clock **193** cycle. Thus, data order multiplexer **180** toggles output **196** between the output of rising edge latch **174** and the output of falling edge latch **176** with each core clock **190** cycle since data order latch **184** is clocked by core clock **190**.

Sample time **220** selects the base range of the DDR-SDRAM data synchronization window. Sample time **220** and memory clock **193** are used to determine whether the output of rising edge latch **174** or the output of falling edge latch **176** is forwarded to configuration section **182** on output **196** with the rising edge of memory clock **193** cycle. Thus, depending on the sample time **220**, the output of rising edge latch **174** may be forwarded through data order multiplexer **180** on the rising edge of memory clock **193** cycle or the falling edge of memory clock **193** cycle. As previously described, the rising and falling edges of strobe signal **152** may be offset from memory clock **193** cycle so the output of rising edge latch **174** may not be available until the falling edge of memory clock **193** cycle. In one embodiment, the base range identified by sample time **220** is either 5 nanoseconds to 15 nanoseconds or 10 nanoseconds to 20 nanoseconds. Sample time **220** determines whether the output of rising edge latch **174** is forwarded on the rising edge of memory clock **193** cycle or the falling edge of memory clock **193** cycle. Since memory clock **193** cycle may not rise and fall at the exact time that strobe signal **152** rises and falls, sample time **220** allows the data signals from rising edge latch **174** and falling edge latch **176** to be forwarded with relation to the rising and falling edges of memory clock **193**. Sample time **220** is a static signal that is set during initial testing of configurable synchronizer **10**. Once sample time **220** is set, it is not generally reset unless system components change or system processing speed changes.

Data order latch **184** synchronizes strobe clock signal **194** with core clock **190**. With each rising edge of core clock **190** cycle, data order latch **184** changes state thereby producing a data order control signal **195** with each core clock **190** cycle. Therefore, data order multiplexer **180** alternates between the output of rising edge latch **174** and the output of falling edge latch **176** with each core clock **190** cycle. Data order latch **184**, strobe clock generator **192**, and their associated input signals may together be referred to as a data order module. The data order module generates the data order control signal **195**.

A clock edge select signal **198** allows configuration section **182** to provide an output signal **200** on the rising edge of core clock **190** or the falling edge of core clock **190**. Clock edge select signal **198** is a static signal that is set on either the rising edge of core clock **190** cycle or the falling edge of core clock **190** cycle during initial system testing. Once clock edge select signal **198** is set, it is generally not reset unless system components are changed.

Output **196** of data order multiplexer **180** is coupled to one input of clock edge select multiplexer **188**. That input provides a different data signal on each rising edge of core clock **190**. The output **196** of data order multiplexer **180** is also coupled to clock edge select latch **186**. Clock edge select latch **186** changes state on the falling edge of core clock **190** as indicated by an inverted core clock **190** signal coupled to the clock input of clock edge select latch **186**. The output of clock edge select latch **186** is coupled to a second input of clock edge select multiplexer **188**. That input provides a different data signal with each falling edge of core clock **190**. Clock edge select latch **186**, clock edge select multiplexer **188**, and clock edge select signal **198** may be referred to as a cycle increment module. The cycle increment module receives a clock edge select signal **198** and forwards the output **196** of data order multiplexer **180** to the output latch **202** on either a rising edge of the core clock **190** cycle or a falling edge of the core clock **190** cycle in response to the clock edge select signal **198**.

Clock edge select signal **198** and sample time **220** allow configuration of synchronizer circuit **44** to quarter cycle granularity thereby optimizing the performance and processing speed of a computer system using configurable synchronizer **10**. Providing configuration of synchronizer circuit **44** in quarter cycle granularity allows a computer system using configurable synchronizer **10** to be run at different speeds and to be margin tested to determine an optimal operating speed for a computer system.

An output latch **202** provides an output signal **154** from synchronizer circuit **44**. Output latch **202** receives as input the output signal **200** from clock edge select multiplexer **188**. Output latch **202** is clocked by core clock **190** thereby forwarding output signal **200** to output signal **154** with each rising edge of core clock **190**.

Referring to FIG. **5**, a timing diagram for configurable synchronizer **10** is generally indicated at **300**. The timing diagram shows the relationship between memory clock **193**, core clock **190**, strobe signal **152**, data signal **150**, strobe disable signal **162**, and data control signal **195**.

Thus, it is apparent that there has been provided, in accordance with the present invention, a configurable synchronizer for double data rate synchronous dynamic random access memory that satisfies the advantages set forth above. Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations may be readily apparent to those skilled in the art and may be made herein without departing from the spirit and the scope of the present invention as defined by the following claims.

What is claimed is:

1. A configurable synchronizer for DDR-SDRAM, comprising:

a strobe select module operable to receive a memory select signal and to pass strobe signals from one or more DDR-SDRAMs;

one or more synchronizer circuits corresponding to data signals passed in parallel by each DDR-SDRAM as indicated by the memory select signal;

wherein each synchronizer circuit includes:

a rising edge latch operable to receive a rising edge data signal from the DDR-SDRAM and to latch the rising edge data signal through the rising edge latch on a rising edge of the strobe signal;

a falling edge latch operable to receive a falling edge data signal from the DDR-SDRAM and to latch the falling edge data signal through the falling edge latch on a falling edge of the strobe signal;

a data signal selector operable to receive a data order control signal and to forward the rising edge data signal from the rising edge latch to an intermediate output on either a rising edge of a memory clock cycle or a falling edge of a memory clock cycle followed by forwarding the falling edge data signal from the falling edge latch to the intermediate output on an opposite edge of the memory clock cycle in response to the data order control signal;

an output latch operable to receive the intermediate output and to latch the intermediate output through the output latch to an output signal on each core clock cycle.

2. The configurable synchronizer of claim 1, further comprising:

a strobe delay module coupled to the strobe select module and operable to receive a strobe delay signal and to delay the strobe signal for a period of time as indicated by the strobe delay signal.

3. The configurable synchronizer of claim 1, further comprising:

a strobe disable module coupled to the falling edge latch and operable to receive a strobe disable signal and to recirculate data from a falling edge latch after receiving a final falling edge data signal in a read burst from the DDR-SDRAM in response to the strobe disable signal, the strobe disable module preventing false data from being latched into the falling edge latch, the strobe disable signal indicating the arrival of the final falling edge data signal in the read burst from the DDR-SDRAM.

4. The configurable synchronizer of claim 1, further comprising:

a cycle increment module coupled to the output latch and operable to receive a clock edge select signal and to forward the intermediate output to the output latch on either a rising edge of the core clock cycle or a falling edge of the core clock cycle in response to the clock edge select signal.

5. The configurable synchronizer of claim 1, further comprising:

a data order module operable to receive the memory clock cycle and a sample time, the data order module further operable to generate a data order control signal on the rising edge of the memory clock cycle for either the latched rising edge data signal or the latched falling edge data signal in response to the sample time, the data order module further operable to generate a data order control signal on the falling edge of the memory clock cycle for the data signal not selected on the rising edge of the memory clock cycle, the sample time indicating which latched data signal should be selected first in the data signal selector.

6. The configurable synchronizer of claim 1, wherein the memory clock cycle is equal to approximately two core clock cycles.

7. The configurable synchronizer of claim 1, wherein the one or more DDR-SDRAMs includes a DDR-SDRAM selected from the group consisting of:

an 8-bit DDR-SDRAM;

a 16-bit DDR-SDRAM; and

a 32-bit DDR-SDRAM.

8. The configurable synchronizer of claim 1, wherein the one or more DDR-SDRAMs includes two 4-bit DDR-SDRAM modules, each DDR-SDRAM module transmitting a strobe signal.

9. The configurable synchronizer of claim 8, wherein the strobe select module is further operable to pass the strobe signal for the DDR-SDRAM to the synchronizer circuits corresponding to the data signals passed by the DDR-SDRAM module.

10. The configurable synchronizer of claim 1, wherein the memory select signal indicates that the one or more DDR-SDRAMs includes a DDR-SDRAM module selected from the group consisting of:

an 8-bit DDR-SDRAM module;

a 16-bit DDR-SDRAM module; and

a 32-bit DDR-SDRAM module.

11. The configurable synchronizer of claim 1, wherein the memory select signal indicates that the one or more DDR-SDRAMs includes two 4-bit DDR-SDRAM modules.

12. The configurable synchronizer of claim 2, wherein the strobe delay signal indicates a delay sufficient to allow the strobe signal to be within a center of a data valid window.

13. The configurable synchronizer of claim 12, wherein the strobe delay signal indicates a delay chosen from the group consisting of: 0 nanoseconds, 0.9 nanoseconds, 1.8 nanoseconds, and 2.7 nanoseconds.

14. A method for synchronizing a DDR-SDRAM with a core clock, comprising:

receiving a strobe signal associated with a DDR-SDRAM module;

receiving a rising edge data signal from the DDR-SDRAM on a rising edge of the strobe signal;

receiving a falling edge data signal from the DDR-SDRAM on a falling edge of the strobe signal;

latching the rising edge data signal on a rising edge of the strobe signal;

latching the falling edge data signal on a falling edge of the strobe signal;

selecting either the latched rising edge data signal or the latched falling edge data signal in response to a data order control signal, the data order control signal alternating between selecting the latched rising edge data signal and the latched falling edge data signal;

latching the selected signal onto a data output signal on each cycle of a core clock.

15. The method of claim 14, further comprising:

delaying the strobe signal for a period of time in response to a strobe delay signal.

16. The method of claim 14, further comprising:

recirculating the falling edge data signal in response to receiving a strobe disable signal indicating that a final falling edge data signal has been received for a read burst.

17. The method of claim 14, further comprising:

delaying the selected signal for one half of a core clock cycle before providing the selected signal to the final latching step in response to a clock edge select signal.

18. The method of claim 14, wherein delaying the strobe signal includes choosing a delay period that allows a strobe signal associated with the data signals to be within a center of a data valid window.

19. The method of claim 14, further comprising:

receiving a memory select signal indicating a size of the DDR-SDRAM module.

20. The method of claim 14, further comprising:

generating a data order control signal from a memory clock cycle and a sample time, the sample time indicating whether the latched rising edge data signal or the latched falling edge data signal should be selected on a rising edge of the memory clock cycle, the data order control signal indicating which data signal to select on the rising edge of the memory clock cycle and on the falling edge of the memory clock cycle, a different data signal being selected on each edge of the memory clock cycle.

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